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Fusion and Technology for Nuclear Safety and Security Department
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OVERVIEW ON NEW HIGH VOLTAGE PULSE MODULATORS IN THE RF POWER SYSTEMS

RT/2017/30/ENEA

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Vincenzo Surrenti

Abstract

Over the last 50 years, the technology of high voltage pulse modulators has undergone remarkable improvements thanks to the use of new semiconductor devices, high integration control systems and the implementation of multicore pulse transformers designed by numerical methods (FEM computing, method of image charges, image current method).
The main advantages of these technological innovations have resulted in:
- *Power systems with efficiencies of up to 99%;*
- *Impulsive output responses with lower rise time and droop voltage;*
- *Increasing output voltages to be able to power radiofrequency tube devices capable of delivering better performance in terms of frequency response, power and efficiency.*

These pulse modulators, once used in limited applications (radar systems, industrial radiofrequency systems), are today used in a wide variety of industrial, medical and research applications, particularly where reliability, stability and versatility are required, thanks to increased performance and to reduced manufacturing costs.
This report will first describe the schemes that are mainly used in the implementation of new pulse modulators and then will be focused on high-voltage modulators based on a pulse transformer. Then, the general block diagram of the above mentioned modulator type will be illustrated and the peculiarities of each subsystem will be described indicating the technological solutions to be used to improve the performances.

Key words: *Power electronics, Solid state modulator, Pulse transformers, Pulse modulation, Pulse circuits, Transformer cores, Pulse power systems, Pulse generation, Pulsed RF power, Klystron-modulator RF power system.*

Riassunto

Negli ultimi 50 anni, la tecnologia costruttiva dei modulatori impulsivi ad alta tensione ha subito notevoli migliorie grazie all'impiego di nuovi dispositivi a semiconduttore, sistemi di controllo ad alta integrazione ed alla realizzazione di trasformatori d'impulso multicore progettati mediante l'ausilio di metodi numerici (FEM computing, metodo delle cariche immagine, metodo delle correnti immagine).
I principali vantaggi ottenuti da queste innovazioni tecnologiche hanno permesso di ottenere:
- sistemi di potenza con efficienze prossime al 99%,
- risposte impulsive in uscita con minori rise time e droop voltage,
- tensioni d'uscita sempre più elevate per poter alimentare dispositivi a tubo per radiofrequenza capaci di fornire prestazioni migliori in termini di risposta in frequenza, potenza ed efficienza.

Questi modulatori impulsivi, che un tempo trovavano impiego in limitate applicazioni (impianti radar, impianti a radio frequenza in campo industriale), oggi vengono impiegati grazie all'incremento delle loro prestazioni ed alla riduzione dei costi in svariate applicazioni industriali, medicali e di ricerca soprattutto laddove è richiesta affidabilità, stabilità e versatilità di funzionamento.
Nel presente rapporto descriveremo preliminarmente quali sono gli schemi prevalentemente impiegati nella realizzazione dei nuovi modulatori impulsivi per concentrare l'attenzione sui modulatori ad alta tensione basati su un trasformatore d'impulso. Quindi verrà illustrato lo schema blocchi generale del suddetto tipo di modulatore descrivendone le peculiarità di ciascun sottosistema e indicando le soluzioni tecnologiche adottate per migliorarne le prestazioni.

Parole chiave: Elettronica di potenza, Modulatori a stato solido, Trasformatori d'impulso, Circuiti impulsivi, Sistemi di potenza impulsivi, Generatori d'impulsi, Potenza RF impulsata, Sistemi di potenza per modulatori RF.

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1 Introduction

In radiofrequency (RF) power plants, the RF signal can be directly generated by a power source or amplified by a low power seed.

In both cases, the power plant involves the use of a tube device, which has the following common elements:

- An electron *gun* or *cathode*,
- A *collector* or *anode* where accelerated electrons are collected.

In the first case, the sources are constituted by tube devices that can generate from the background noise and self-sustaining the natural oscillations for which the tube has been realized. The *magnetron*, the *gyrotron*, the *CARM* belong to this class of devices.

In the second case, the tube device, by means of an electron beam *velocity modulation* mechanism produced by the gun, is capable of amplifying a RF signal. The *klystron* and the *traveling wave tube* belong to this class of devices.

There are also other types of power tube devices that are used in radiofrequency power plants, as amplifiers, that amplify a source RF signal by means of a *current modulation* mechanism. The *planar triode*, the *pentode*, the *tetrode* and the inductive output tube belong to this class of devices.

All these devices in order to be able to operate impulsively must be powered by a pulse modulator. There are many applications where it is required the use of RF sources operating impulsively for industrial, medical and research. However, every type of application is characterized by a particular power and pulse duration.

In the case of industrial use these systems can feed:

- radar installations,
- radiofrequency ovens,
- radiographic equipment,
- sterilization systems for radiofrequency and accelerated electrons,

and it is therefore important that the pulse modulator has the highest efficiency and the greater power.

In the case of medical use, these systems can feed:

- radiogenic sources,
- source for the production of radiotherapy drugs,
- hadron-therapy machines

and in this case, the pulse modulator requires a stable response in terms of *rising time* and *droop voltage*.

Finally, in the case of use in research facilities, these modulators can feed for example:

- long linear colliders,
- nuclear fusion devices.

The demand for the pulse modulator in this case is twofold, i.e. it is necessary to ensure *stable responses* and an *overall efficient* system. In this report, new types of pulse modulators for RF devices will be examined, mainly made with solid-state switching devices.

2 State of the art of the solid state High Voltage Modulator

In the last 50 years the development of modern high-voltage modulators has changed considerably, basically thanks to the progress made in the following areas:

- integration of programmable devices such as ARM, FPGA, etc.
- development of new power solid-state devices that can operate with maximum operating voltages around the thousand volts and rated currents around the thousand amperes.

This progress have led to a change in state of the art of modern High-Voltage Modulators. Today modern high voltage modulators are to be classified according to the following two parameters: pulse length and used power. In fact, in function of the above parameters they find a very precise application as is illustrated in *Fig. 1*.

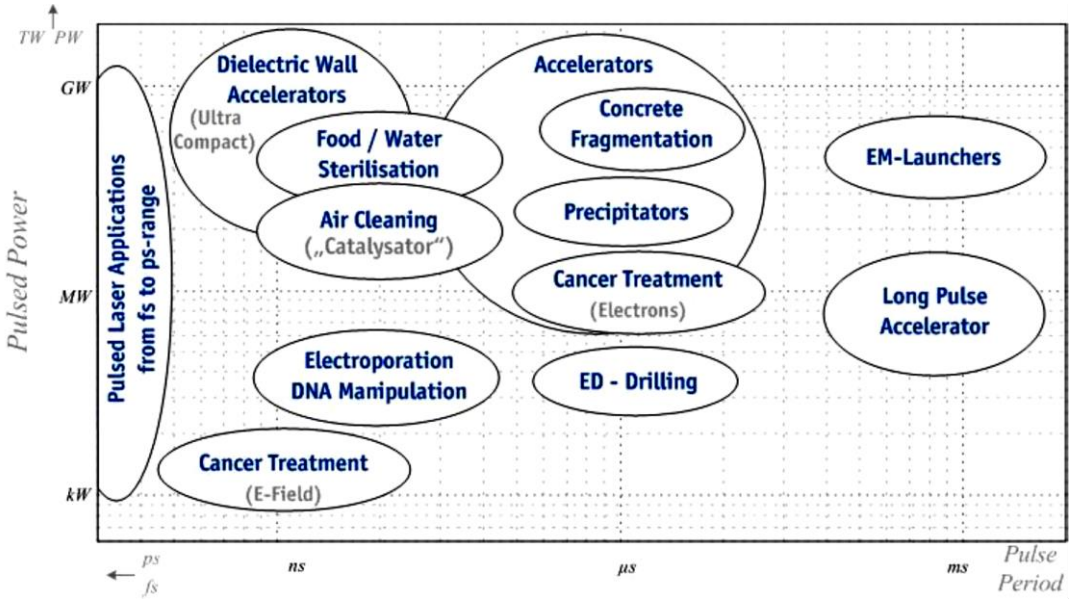


Fig. 1 *Pulsed power vs pulse length for typical application*

According to the classification shown in the *Fig. 1* and according to the construction technology the modern solid state high voltage pulse modulators can be divided into the following three large families:

- Short pulse modulator,
- Mid-range pulse modulator,
- Long pulse modulator.

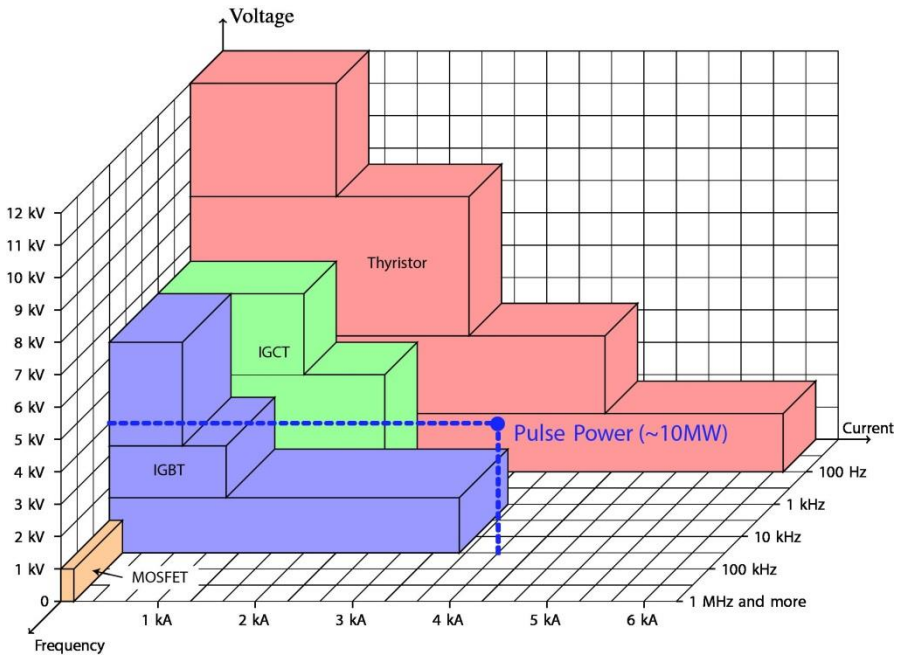


Fig. 2 *Solid state switches type vs frequency, current and voltage*

Fig. 2 shown today's operating limits of the solid state devices used in the production of modern pulse modulators. The above graph justifies the use of Thyristors and IGCTs in long pulse modulator and the use of IGBTs and MOSFETs in the mid-range and short pulse modulator. However, the use of this last type of devices in large power plants involves the use of more complex and expensive circuit configurations to overcome the limited operating range in voltage and current.

In design phase of high voltage pulse modulators, it is necessary to reduce the operating voltage of the electronic devices used as switches with respect to what is indicated by the manufacturer to increase the mean time to failure; this reduction in the operating voltage should be weighted according to the height of installation of the system. Indeed, in these devices that operate for long intervals of time in reverse bias, the avalanche breakdown phenomenon as result of swarms of cosmic rays in the reverse bias region becomes all the more probable, the higher is the working height of the plant and the more extended is the reverse region (that is, the higher the reverse bias voltage). Reducing the operating voltage of the switch involves their use in chains connected in series and in the design phase it is necessary that particular attention is made to the interconnection and command mode to avoid extra-tension in the opening phase.

Another requirement to be met, in case it is wanted to realize a pulse modulator which operates at high power, the switching devices must be connected in parallel so as to respect the current operating limits.

Today most of the pulse modulators, to improve the conversion efficiency of the switching devices, are controlled by suitable drivers operating in ***boundary conduction mode*** (BCM). In this way the inductive current controlled by the switching device flows in a discontinuous mode, the main benefit is a reduction in

the magnetic energy stored by the inductor or transformer with a consequent reduction in the size, weight and power losses of the latter.

3 Topological scheme of the solid state High Voltage Modulator

There are two possible realization for a solid-state modulator, a *Marx generator* and a *pulse-transformer-based* solution.

The *Marx generator* (cfc. *Fig. 3*) is based on the principle of charging capacitors in parallel for a period and, in a subsequent period, to connect the capacitors in series to create a higher voltage. The classical Marx generator uses spark gaps to connect capacitors in series and to create a single high-voltage pulse. Nowadays, modern topologies based on the same principle can be realized with solid-states switches. The modularity of this type of converter allows to make connections in series and in parallel between modules in order to meet all requirements in terms of voltage and current which also show a high level of reliability, availability and maintainability. The main disadvantage of this type of modulator is the high energy level stored, by requiring costly systems for safe disposal in case of short circuit (electro-optic circuit devices for electrostatic decoupling of the electronic drive circuit of the switches). Just for the abovementioned disadvantages, this type of converter is adopted to realize steady-state converters dc-dc or long pulse modulator.

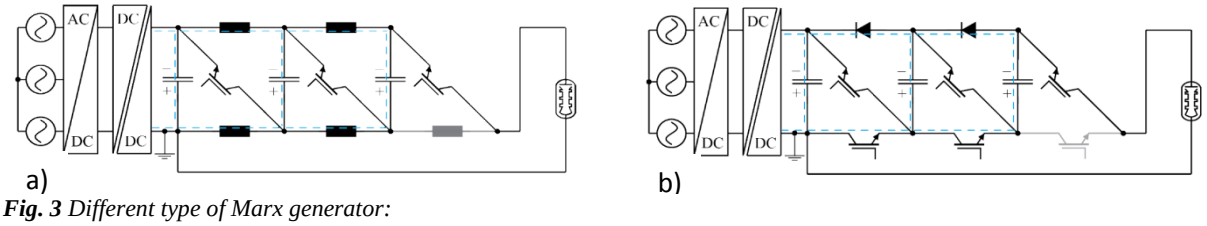


Fig. 3 *Different type of Marx generator:*
a) the capacitor is charged by inductor and resistor b) the capacitor is charged by switch and diode

In a *pulse-transformer based* modulators, thanks to the use of a transformer the switches can be operated at a lower voltage. In addition, less switches are required, because there is no series connection necessary to achieve the output voltage.

Pulse-transformer-based modulators can be divided into three different categories:

- *transformers with a single core*,
- *transformers with multiple cores*,
- *and transmission-line transformers*.

A *single-core transformer* consists of one magnetic core and two or more windings. *Transformers with multiple cores* are realized in different configurations. The simplest solution is connecting multiple transformers in series or in parallel. A parallel connection of multiple pulse transformers does not result in

any benefit compared with a solution, where multiple switches are connected in parallel on the primary side of a single-core transformer. Connecting multiple transformers in series is more useful. The current on the primary side is given by the current on the secondary side and the turns ratio. Therefore the series connection guarantees equal currents on the secondary side of all transformers, resulting in equal currents on the primary side if the transformers have the same turns ratio. The load current is equally shared between the semiconductor switches.

The series connection of multiple transformers can be improved by enclosing all cores with one secondary winding, instead of an individual secondary winding for each core.

The third possible structure is a ***transmission-line transformer***. In such transformers, multiple transmission lines are connected to a common source at one end and in series at the other end of the line [4]. These types of structure are referred to as ‘‘ line-type” pulsers because the energy-storage device is essentially a lumped-constant transmission line. Since this component of the line type pulser serves not only as the source of electrical energy during the pulse but also as the pulse-shaping element, it has become commonly known as a “ *pulse-forming network*,” *PFN*. There are essentially two classes of *pulse-forming networks*, namely, those in which the energy for the pulse is stored in an electrostatic field in the amount $\frac{1}{2}CV^2$ and those in which this energy is in a magnetic field in the amount $\frac{1}{2}LI^2$. Often, coaxial cables are used as transmission lines. To improve the low-frequency response, the cables are wound around a magnetic core. Other times the lumped-constant transmission line consist of inductances and condensers which may be put together in any one of a number of possible configurations. The configuration chosen for the particular purpose at hand depends on the ease with which the network can be fabricated, as well as on the specific pulse characteristic desired. Anyway, it is realized the transmission line, the impedance must be matched to the load impedance for maximum power transfer. The main disadvantage of this type of modulators is the setup of the forming network in accord to the applied load.

Among the described modulators the most diffused in the construction of high voltage pulse generator with pulses of duration up to the millisecond is the pulse modulator based on the transformer in the version in single or multiple magnetic cores. Its development is due to the ease with which its design can be adapted to any type of RF source or load.

The general layout of a high voltage pulse transformer-based modulator consists of the following subsystems:

- a galvanically isolated ac/dc converter with a Power Factor Correction (PFC)
- a Charging Unit
- a Primary Bank of energy storage
- one or more Pulse Generator (included the pulse transformer)
- a possible Bouncer subsystem

interconnected as shown in *Fig. 4*.

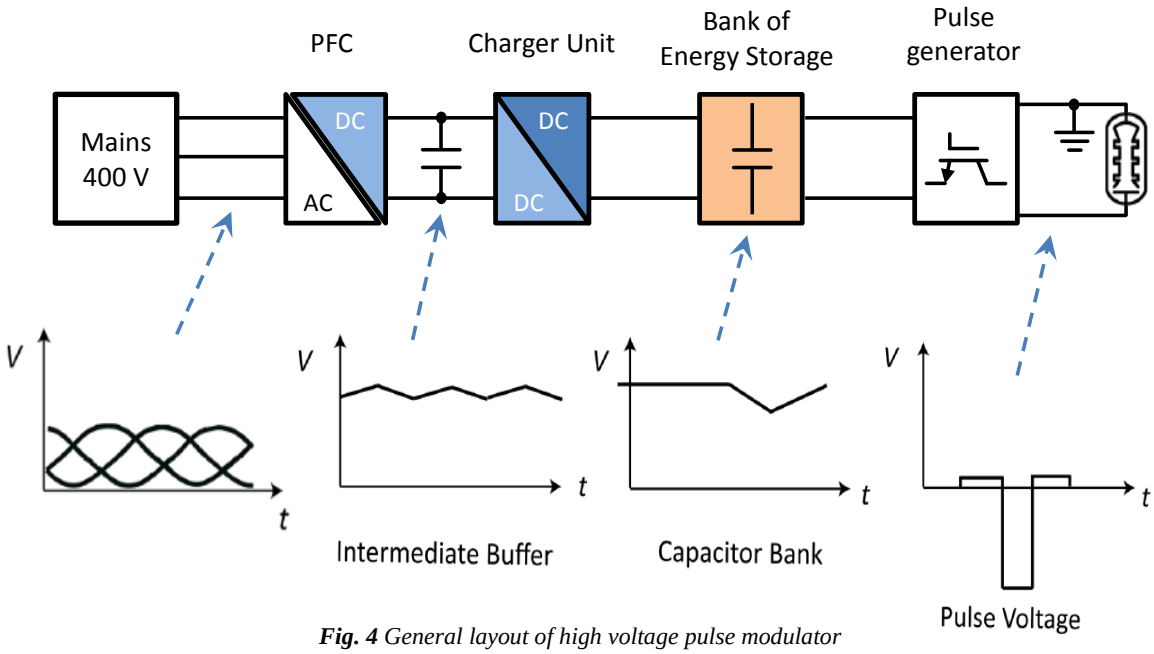


Fig. 4 *General layout of high voltage pulse modulator*

The following paragraphs have been divided for each subsystem in order to motivate their use, describe the principle of operation, indicating the upgrades that have improved efficiency, and that have allowed their use even when the design specifications are difficult to meet.

4 Distribution network

The preliminary study of the feasibility of a pulse modulator object of the present documents contemplate its insertion in an electrical distribution system, subject to the Italian laws. In particular, the point of access to the electricity distribution network is constituted by a secondary substation supplied in MV (Medium Voltage), provided with at least a MV / LV (Low Voltage) transformer dedicated to the distribution network (law's norms CEI 0-16 art. 3.2, CEI 0-21 art. 3.2, CEI 64-8/2 art. 21.8). The MV / LV transformer of that distribution station is generally made up of a three-phase transformer with internal ΔY connection and the following conversion ratio 20kV / 400V.

The type of the neutral connection and the grounds connection to be taken into consideration is that of a TN-S system. For this type of system it is provided the separate use of neutral and protection conductors, therefore the security is related to the efficiency of the neutral and ground network.

It must be remembered that the legislative norms for TN systems contemplate a different type of protective devices for the direct cables contact and for indirect contact. In fact, in the first case it is provided the use of devices that monitor the maximum operating current of the plant and which ensures a inversely proportional to the contact current intervention time. For indirect contacts is contemplated instead the realization of the ***ground systems*** that consist of sinks, ground conductors and equipotential conductors and a system which monitors the current difference between the phase current and the neutral current.

This premise is essential in the choice of design as it will ensure the integration of the system into the electrical distribution network, making it easier to design the diagnostic system for detecting plant failures and operations to be used to protect the plant.

5 PFC and level tranformer

The first subsystem that will be described is the *Power Factor Correction* (***PFC)***. The PFC performs the following tasks:

- to ***correct the power factor*** shown by the modulator to the power grid,
- ***uncouple galvanically*** the charge unit from the main distribution network,
- to provide an ***adequate output voltage*** to the pulse generator.

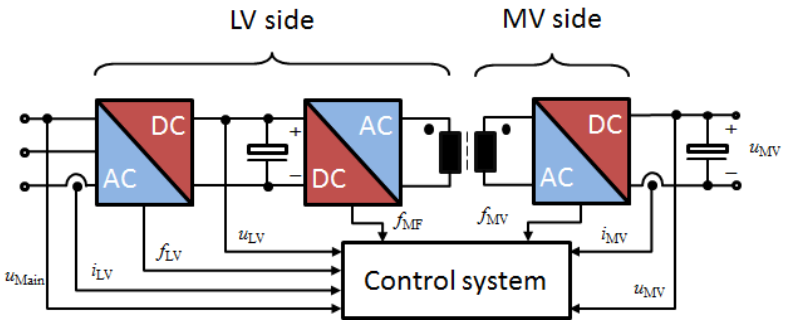


Fig. 5 *Typical layout of the Power Factor Correction*

In *Fig. 5* is shown a typical layout where it is possible identify the following subsystem:

- An AC / DC converter: that in addition to providing a continuous output voltage will allow to correct the power factor shown to the distribution network.
- A DC/DC converter: consists in turn of two subsystems, a DC/AC converter and an AC/DC converter (full bridge type) galvanically decoupled by the transformer which also shifts the level of the PFC output voltage.
- An integrated control system that manages all the subsystems in order to reduce the *Total Harmonic Distorsion* (THD) of the current request to the distribution network, and provide the predetermined output voltage. Finally, the control system is able to handle the direction of the energy flow so that it can be recovered when the modulator is in standby mode or if it is necessary to handle a fault (load side).

Correct the power factor involves modifying the input current waveform of the power supplies in such a way that the distributor mains always provide a real power to the modulator. Another reason to employ PFC in many of today's power supplies is to respect the legal requirements. Today, electrical equipment in Europe must comply with the IEC 61000-3-4 and IEC 61000-3-12 (limitation of harmonic currents injected

into the public supply system). This requirements specify the maximum amplitude of line-frequency harmonics up to and including the 39th harmonic.

Minimal R_{sce}	Admissible individual harmonic current I_n/I_1 [a] %						Admissible harmonic current distortion factors %	
	I_3	I_5	I_7	I_9	I_{11}	I_{13}	*THD*	*PWHD*
33	21,6	10,7	7,2	3,8	3,1	2	23	23
66	24	13	8	5	4	3	26	26
120	27	15	10	6	5	4	30	30
250	35	20	13	9	8	6	40	40
≥ 350	41	24	15	12	10	8	47	47
The relative values of even harmonics up to order 12 shall not exceed 16/*n* %. Even harmonics above order 12 are taken into account in *THD* and *PWHD* in the same way as odd order harmonics.								
[a] I_1 = reference fundamental current; I_n = harmonic current component.								

Tab. 1 *IEC 61000-3-12 requirements for balanced three-phase equipment*

Minimal R_{sce}	Admissible individual harmonic current I_n/I_1 [a] %				Admissible harmonic current distortion factors %	
	I_5	I_7	I_{11}	I_{13}	*THD*	*PWHD*
33	10,7	7,2	3,1	2	13	22
66	14	9	5	3	16	25
120	19	12	7	4	22	28
250	31	20	12	7	37	38
≥350	40	25	15	10	48	46
The relative values of even harmonics up to order 12 shall not exceed 16/*n* %. Even harmonics above order 12 are taken into account in *THD* and *PWHD* in the same way as odd order harmonics.						
[a] I_1 = reference fundamental current; I_n = harmonic current component.						

Tab. 2 *IEC 61000-3-12 requirements for equipment other than balanced three-phase*

In *Tab. 1* and *Tab. 2* is shown in tabular form the requirements for different types of equipment as a function of the *short-circuit ratio* (Rsce) or :

$$R_{sce\ min} = \frac{V}{Z \cdot I_{eq}}$$

where V is the grid line voltage, Z is the supply output impedance and I_{eq} is the target line current.

Power factor correction is simply defined as the ratio of real power to apparent power, or:

$$PF = \frac{Real\ Power}{Apparent\ Power} \quad \begin{matrix} (expressed\ in\ Watts) \\ (expressed\ in\ VA) \end{matrix}$$

where the real power is the average, over a cycle, of the instantaneous product of current and voltage, and the apparent power is the product of the rms value of current per the rms value of voltage. If the load is composed of resistive, capacitive and inductive elements and all are linear (invariant with current and voltage). In the case which the current and voltage are sinusoidal and in phase (resistive load), the power factor is 1.0 while if both are sinusoidal but not in phase, the power factor is the cosine of the phase angle.

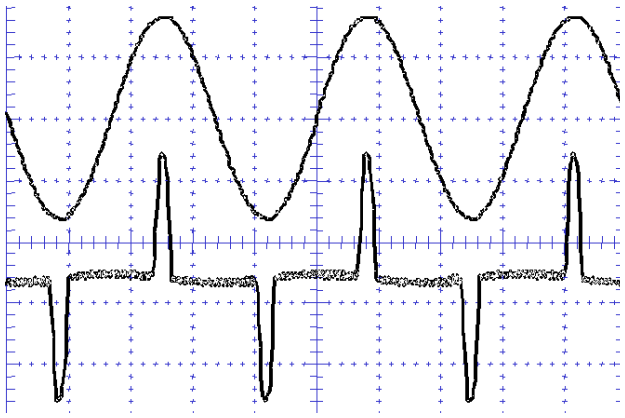


Fig. 6 *Input characteristics of a typical switched power supply without PFC.*

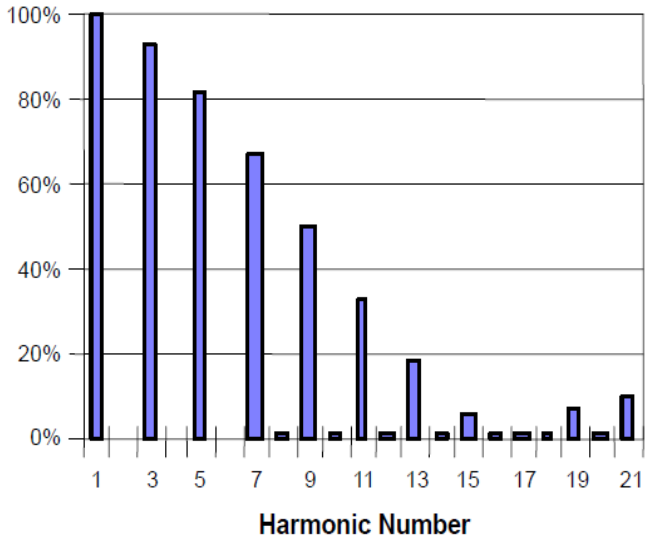


Fig. 7 *Harmonic content of the current waveform in Fig. 6*

The solid state modulator present nonlinear impedance to the mains. The input circuit usually consists of a half-wave or full-wave rectifier followed by a storage capacitor. This latter elements is able to maintain approximately to the peak sinusoidal input voltage until the next peak will arrive to recharge the capacitor. In this case current is drawn from the input only at the peaks of the input waveform, and this pulse of current must contain enough energy to sustain the load until the next peak.

The current and voltage are perfectly in phase (*Fig. 6*) , in spite of the severe distortion of the current waveform. Applying the "cosine of the phase angle" definition would lead to the erroneous conclusion that this power supply has a power factor of 1.0.

However the harmonic content of the current waveform (*Fig. 7*) shows the presence of the even harmonics with not negligible amplitude. Since only the fundamental component produces real power, while the other harmonics contribute to the apparent power, the actual power factor is well below 1.0. This deviation is represented by a term called ***distortion factor*** and is primarily responsible for the non-unity power factor in ***switched power supply*** (SPS).

The general equation governing the relationship between the real power and apparent power is given by:

$$< P_{in} > = \widehat{V_{in}}\widehat{I_{in}}\cos\varphi\cos\theta$$

where $\widehat{\mathbf{V}_{\mathbf{in}}}$ is the rms input voltage, $\widehat{\mathbf{I}_{\mathbf{in}}}$ is the rms input current, $< \mathbf{P_{in}} >$ is the real power expressed in Watt , $\widehat{\mathbf{V}_{\mathbf{in}}}\widehat{\mathbf{I}_{\mathbf{in}}}$ is the apparent power expressed in VA, $\boldsymbol{cos\,\varphi}$ is the displacement factor coming from the phase angle φ between the voltage and current waveforms and $\boldsymbol{cos\theta}$ is the distortion factor.

Therefore it is preferred to define the power factor through the following relation:

$$PF = \lambda = \frac{1}{\sqrt{1+THD_i^2}} cos\varphi \qquad THD_i = 100 \cdot \sqrt{\sum_{p=2}^{\infty} \frac{I_p^2}{I_1^2}}$$

where with $\boldsymbol{THD_i}$ denotes the total harmonic distortion of the input current to the power converter.

In the case of three-phase distribution networks, as always two diode at a time carry current to the converter except in the commutation interval, this means that the conduction angle at most will 60° at which correspond a relatively high low-frequency harmonic content or a THDi ≈ 30%.

In order to avoid voltage distortions resulting from voltage drops across the inner (inductive) mains impedance or the excitation of resonances in the distribution grid a THD_i < 5% at rated power is often required.

This network quality can only be achieved with rectifier systems based by active power factor correction (PFC). A further important aspect of the use of active (PFC) rectifier systems is the possibility to control the output dc voltage to a constant value, independent of the actual mains voltage. A converter stage on the output side can be dimensioned to a narrow voltage range. The mains voltage range must be considered only for the dimensioning of the rectifier stage (the delivery of a given rated power, e.g., at half of the input voltage, leads to a doubling of the input current that must be handled by the power semiconductors, passive power components and the EMI filter).

Therefore the requirements placed on active PFC rectifier systems can be summarized as follows:

- sinusoidal input current according to regulations regarding the mains behavior of three-phase rectifier systems (EN 61000-3-2 if < 16 A, 61000-3-4 if > 16 A); in industry, however, typically independent of the concrete application, a THD_i < 5% is required (at the rated operating point);
- ohmic fundamental mains behavior ($\cos\varphi$ > 0.99);
- regulated output voltage; depending on the required level of the output dc voltage relative to the mains voltage, a system with boost-, buck-, or buck–boost-type characteristic has to be provided;
- handling of a mains phase failure, i.e., for interruption of one mains phase, continued operation at reduced power and unchanged sinusoidal current shape should be possible;
- unidirectional power flow, perhaps with (limited) capability of reactive power compensation;
- compliance with specifications regarding electromagnetic, especially conducted interference emissions by means of suitable EMI filtering.

An approximately sinusoidal mains current and/or partial elimination of low-frequency harmonics in the input current is only obtainable with multipulse systems, i.e., for 12-,18-, or 36-pulse rectifier circuits. This type of PFC is grouped in the class of ***Passive system***.

Integrating the passive system with in cascade power devices that actively control the flow of power it is possible improve the control of the sinusoidal mains current and also adjust the output voltage within certain limits. Such type of PFC is classified as a ***Hybrid system***.

Conversely, if the integration of the power semiconductors takes place inside of each leg of the bridge, the control of switching of these devices will be certainly more complex and therefore in this case the type of PFC will be grouped in the ***Active PFC system.***

The choice of the particular type of PFC, depending on unavoidably from the point of view of the effectiveness in reducing the total harmonic distortion of the input current and in the regulation capability of the output voltage, furthermore it depends on the circuital and control complexity and consequently by the cost of implementation.

The best type of PFC is a particular Active PFC system called Hybrid third harmonic current injection-Active Filter Rectifier.

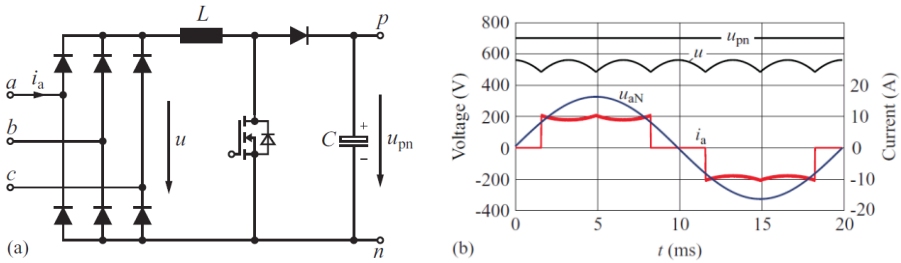


Fig. 8 *Three-phase extension of the boost type PFC* ***:*** *a) system structure and b) corresponding mains voltage and mains current if the dc-dc boost converter stage operates in continuous conduction mode (CCM)*

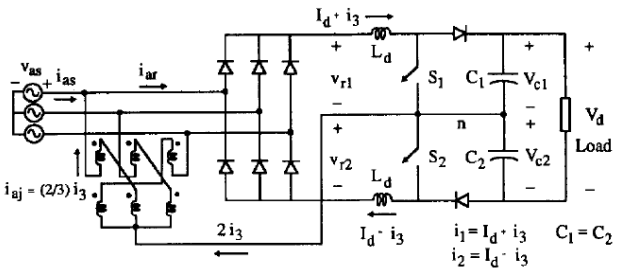


Fig. 9 *Schema of the Hybrid third harmonic current injection-Active Filter Rectifier with the relative current distribution*

This latter is a variant of the boost-type PFC rectifier that over obtain a limited regulation of the output voltage shows good performance from the point of view of the harmonic distortion of the input current.

In fact, the boost-type PFC rectifier (chain in cascade of two stage: three-phase bridge and a boost-converter dc-dc) is capable to providing a harmonic distortion of input current not less than 30%.

In *Fig. 9* is shown the basic configuration of the conventional current injection topology for a three-phase diode rectifier that fed a load.

It consists of two stages. The first stage is a six-pulse, diode-bridge rectifier. The second stage consists of two step-up dc-dc (boost) converters which modulate the current in the dc-link to be ($I_d + i_3$) and ($I_d - i_3$).

The I_d current is the dc component of the current and i_3 is the third-harmonic modulation current flowing in the dc-link inductors.

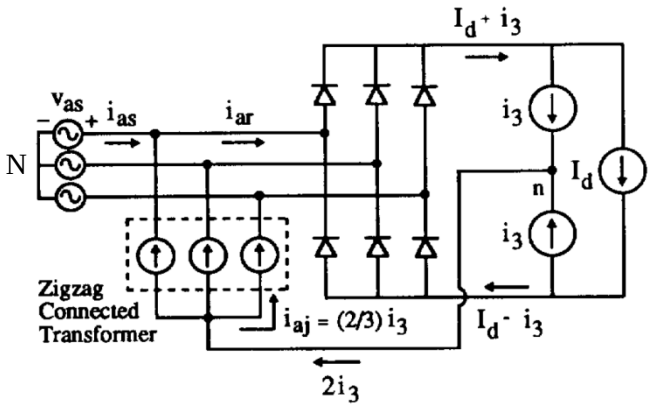


Fig. 10 *Simplified representation of the Hybrid third harmonic current injection-Active Filter Rectifier*

A simplified diagram of the PFC in which is visible the flow of the third harmonic current is illustrated in *Fig. 10*. The two step-up dc-dc converters on the dc side are represented by third-harmonic current sources. The currents from these two sources add up, at the midpoint *n*, and the sum $2\ i_3$ is circulated through the ac side of the rectifier by a zigzag autotransformer.

The zigzag connection presents a high magnetizing impedance for the fundamental frequency voltages and a low leakage impedance for the third-harmonic (zero-sequence[A1]) current. The total third-harmonic current $2\ i_3$ splits equally in the three legs of the transformer and constitutes the current i_{aj} flowing in each leg.

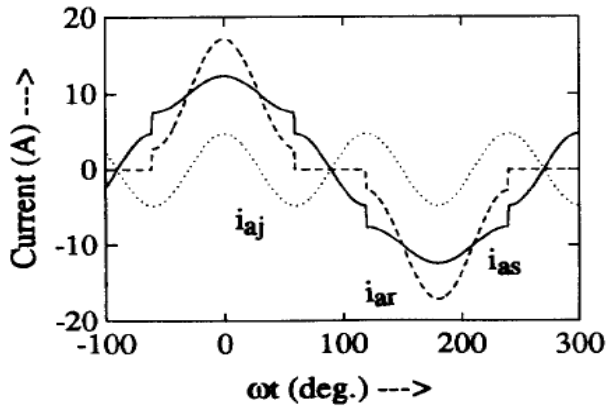


Fig. 11 *Waveforms of the currents in the simplified circuit of Fig. 10*

This circulating current i_{aj}, subtracts from the input current i_{ar}, to the diode-bridge rectifier, and results in the line current i_{as}, as shown in *Fig. 11*. The line current i_{as}, seen to approach the sinusoidal wave-shape and has reduced harmonic content.

The use of an zigzag autotransformer ensures that, whatever the value of the network inductance L_s, the third harmonic component of the current injected on the star point, thank a low leakage impedance of the autotransformer, implies a negligible potential difference V_{Nn}, in the presence of zero-sequence current.

[A1] In a polyphase networks a set of balanced phasors equal in magnitude and in phase with each other and without rotation sequence is known as a ***zero sequence***.

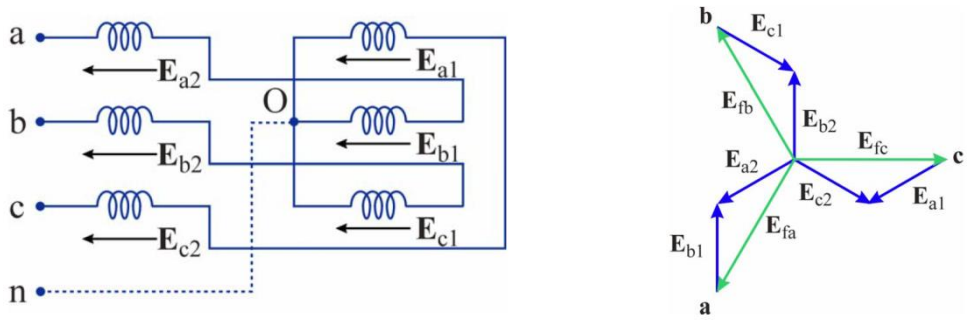


Fig. 12 *Schema of windings interconnection a zig-zag autotransformer and relative representation of the phasors tension*

In *Fig. 12* is shown the relationship between the line voltages and phase voltages in a zigzag autotransformer. The third harmonic current (zero sequence) injected into the star point of the autotransformer will be represented on the same plane as the vector sum of two phasors rotating in the opposite direction. In this case the current flowing in each branch can not to be decomposed in a rotary triplet but in a triplet of zero-sequence components.

This subsystem as well as reducing the harmonic content of the line current is used to adjust the output voltage. The controller of the aforementioned PFC is shown in *Fig. 13*. The reference value $I_{d,ref}$ the dc-link current for each step-up dc-dc converter is obtained by comparing the measured dc bus voltage V_d with a reference value in the steady state, $I_{d,ref}$ for both the step-up dc-dc converters are equal. The magnitude and phase of the modulating current reference $i_{3,ref}$ are obtained from the line voltages and $I_{d,ref}$ so as to minimize the line current harmonics. For proper operation of the circuit, the dc voltage at the output of each step-up dc-dc converter must be equal.

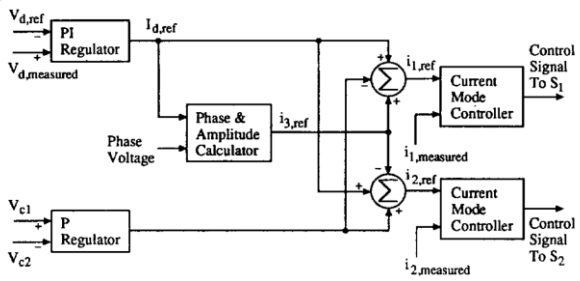


Fig. 13 *Block diagram of the controller.*

This is achieved by comparing the output voltage of the two dc-dc converters and using a negative feedback to equalize them as shown in *Fig. 13*.

The input voltage to each of the two step-up dc-dc converters must always remain positive to ensure proper operation. The voltage at the midpoint ***n*** of the output dc bus is given in phasor notation as

$$\overrightarrow{V_n} = \frac{2}{3}\overrightarrow{Z_3}\overrightarrow{I_3}$$

where $\overrightarrow{Z_3}$ is the impedance of the zigzag transformer at the third-harmonic frequency.

Typical THD values that can be obtained with this type of PFC are 4.25%.

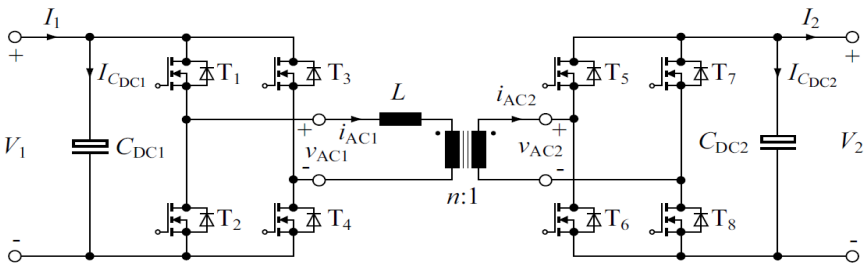


Fig. 14 *Dual Active Bridge (DAB) converter topology*

The regulation index of the active PFC system output voltage, however, is not able to provide sufficient voltage to the next stage. In fact, the boost converter that will feed the bank of capacitors interconnected to the pulse generators in interleaved mode will provide output voltage a little higher than the input so that this meets the specifications required in stability and repeatability. Since this voltage is about equal to the maximum reverse voltage polarization of the switches in the pulse generators, the Active PFC system is generally followed by a DC / DC elevator converter stage which will achieve the desired output voltage value and galvanically decouple the PFC from the next stage (boost converter). Among the possible DC/DC converters has chosen a Dual Active Bridge (DAB). The Single-phase Dual Active Bridge (DAB) converter (*Fig. 14*) contains two voltage sourced full bridge circuits or half bridge circuits (or even push-pull circuits) and a HF transformer. The reactive network simply consists of an inductor L connected in series to the HF transformer; hence, the DAB directly utilizes the transformer stray inductance. Due to the symmetric circuit structure, the DAB readily allows for bidirectional power transfer.

This inherent ability of the converter allows to recover part of the energy stored by the capacitors bank of the pulse generators to transfer it to the capacitor bank immediately to the PFC output. The main advantage of the DAB are the low number of passive components, the evenly shared currents in the switches, and its soft switching properties. With the DAB converter topology, high power density is feasible.

However, the waveforms of the transformer currents $i_{AC1}(t)$ and $i_{AC2}(t)$ highly depend on the actual operating point (i.e. V_1, V_2, and the output power P_{out}); for certain operating points, very high transformer RMS currents result. Moreover, high maximum capacitor RMS currents I_{CDC1} and I_{CDC2} occur.

Given the level of tension on the medium voltage side (MV) the circuit configuration that will be taken in examination provides for the use of IGBTs in place of the MOSFETs for the capacity that have the first in working with voltages in the range of kilovolts. The depicted scheme (*Fig. 14*) provides the use of a controller that operates in Triangular Current Mode (TCM).

This type of circuit configuration allows to define the direction of power transfer and also is able to implement the ***soft-switching*** technique widely used in DC/DC converters of the latest generation with IGBT switches where the switching losses and EMI associated with hard-switching operation (*Fig. 15*. a) can be

significant problem. The term "***soft-switching***" in power electronics refers to various techniques where the switching transitions are made to be more gradual to force either the voltage or current to be zero while the switching transition is being made. EMI is reduced by soft-switching because the switching transitions from on to off and vice versa are gradual and not sudden (*Fig. 15*. b).

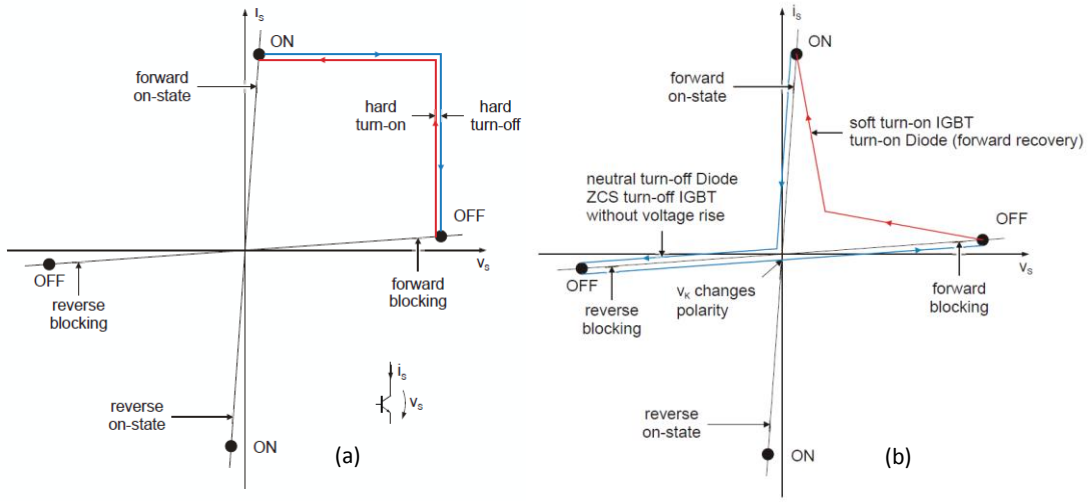


Fig. 15 *(a)Operating point characteristic of switch current and voltage for hard switching,*
(b) Operating point characteristic of switch current and voltage during soft/resonant switching as ZCS

Switching losses are reduced since the power dissipated in a switch, while a switching transition made, is proportional to the overlap of the voltage across the switch and the current flowing through it.

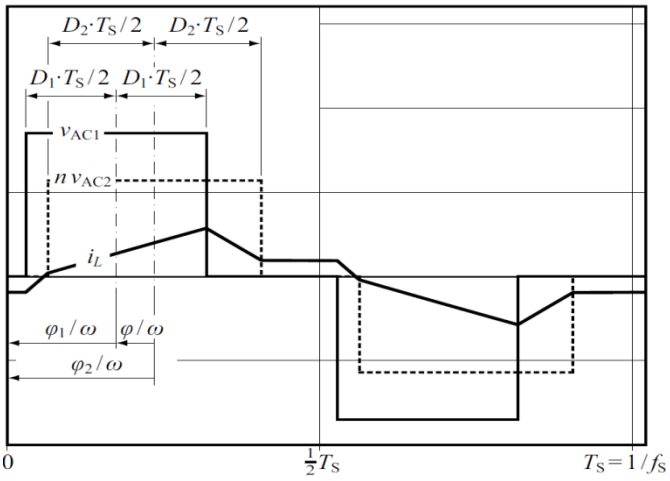


Fig. 16 *The 4 DAB control parameters: $\phi = \phi_2 - \phi_1$ denotes the phaseshift between v_{AC1} and v_{AC2}, D_1 and D_2 are the respective duty cycles, and f_S is the switching frequency.*

Soft-switching forces either the voltage or the current to be zero during the time of transition; therefore there is no overlap between voltage and current and (ideally) no switching loss. There are two types of soft-switching: zero-voltage switching (ZVS) and zero-current switching (ZCS). Although there are many ZVS and ZCS techniques, there are general principles associated with each type. A switch can be made to operate with ZCS if an inductor is added in series to it. The semiconductor switch can turn on with ZCS because the inductor limits the rise in current so that the

current flowing through the switch is almost zero as the device is being turned on.

The switch can turn off with ZCS if a negative voltage is somehow impressed across the inductor-switch combination so that current falls to zero at a gradual rate due to the inductor.

The power level of the DAB converter is typically adjusted using one or more out of the 4 control parameters depicted in *Fig. 16* :

- the phase shift, φ, between $v_{AC1}(t)$ and $v_{AC2}(t)$ with $-\pi < \varphi < \pi$,
- the duty cycle, D_1, of $v_{AC1}(t)$ with $0 < D_1 < 1/2$,
- the duty cycle, D_2, of $v_{AC2}(t)$ with $0 < D_2 < 1/2$, and
- the switching frequency f_S.

The most common modulation principle, the so called phase shift modulation, operates the DAB with a constant switching frequency and with maximum duty cycles, $D_1 = D_2 = 1/2$; it solely varies the phase shift ϕ in order to control the transferred power.

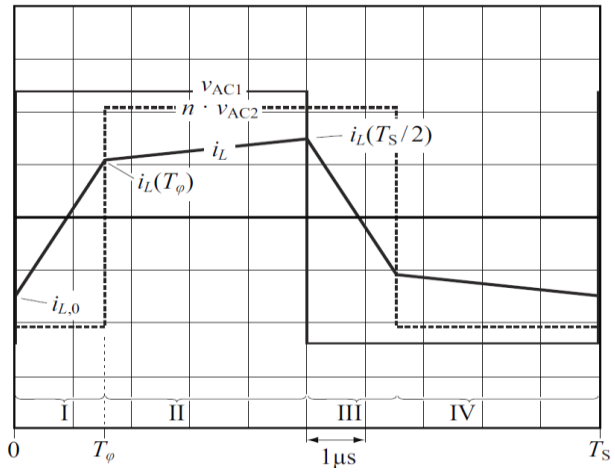


Fig. 17 *Transformer voltages and inductor current for phase shift modulation*

During steady-state operation, the voltages $v_{AC1}(t)$ and $v_{AC2}(t)$ and the inductor current repeat every half-cycle with reversed signs since the phase shift time T_ϕ and the DC supply voltages V_1 and V_2 remain the same during the first and during the second half-cycle (time intervals I, II and III, IV in *Fig. 17*, respectively).

For the calculation of the transferred power, therefore, only the first half-cycle (intervals I and II) needs to be considered. Due to the half-cycle symmetry and with $T_\varphi = \varphi/(2\pi f_s)$

$$i_{L,0} = \frac{\pi(nV_{AC2} - V_{AC1}) - 2\varphi n V_{AC2}}{4\pi f_s L}$$

results for positive phase shift, $0 < \varphi < \pi$, and a similar result is obtained for negative phase shift, $-\pi < \varphi < 0$.

The transferred power results :

$$P = \frac{nV_{AC1}V_{AC2}\varphi(\pi - |\varphi|)}{2\pi^2 f_s L}$$

for each value of the φ will be :

- P > 0 denotes a power transfer from the HV to the LV port and
- P < 0 denotes a power transfer from the LV to the HV port.

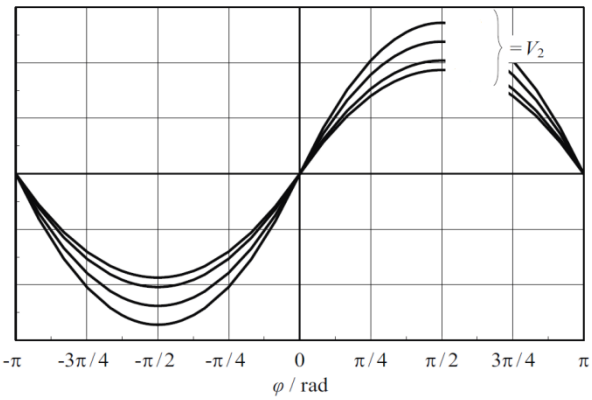


Fig. 18 *Transferred power vs the phase shift for the DAB DC/DC converter*

The achieved power transfer for the DAB converter is depicted in ***Fig.*** *18* and shows a maximum for a certain phase shift angle; the maximum power transfer is analytically evaluable by solving the following equation, $\partial P/\partial\phi=0$, that is :

$$|P_{max}| = \frac{nV_{AC1}V_{AC2}}{8f_sL} \quad \text{for} \quad \varphi = \pm\pi/2$$

This circuit configuration, however, offers the alternative types of modulation that changing the duty cycles of $v_{AC1}(t)$ and $v_{AC2}(t)$, well as the current waveform, allow to reduce the RMS value of the current flowing in the transformer / inductor especially on the side at low voltage and at the same time reducing the switching losses.

Fig. 19 shows a typical trend of the duty cycle of $v_{AC1}(t)$ and $v_{AC2}(t)$ for which the RMS current of the inductor has the minimum value versus the transferred power level.

Having regard to the modest values of the average power that the modulator should handle the DC/DC converter must necessarily operate in triangular current mode. Therefore the design choices of the DC / DC converter will be focused to determine the optimal modulation in the case where it operates in triangular current mode with $V_1 > nV_2$.

In the triangular current mode modulation (*Fig. 20*.

a) the LV side full bridge solely switches at zero transformer current causing low switching losses but the HV side full bridge switches zero transformer once per half period causing high switching losses.

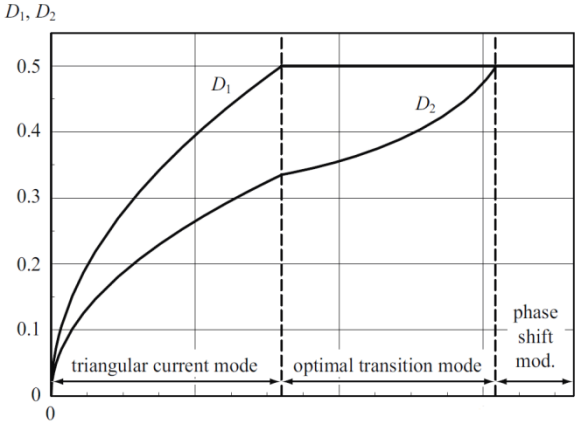


Fig. 19 *Duty cycles D1 and D2, which minimize the inductor RMS current versus the transferred power*

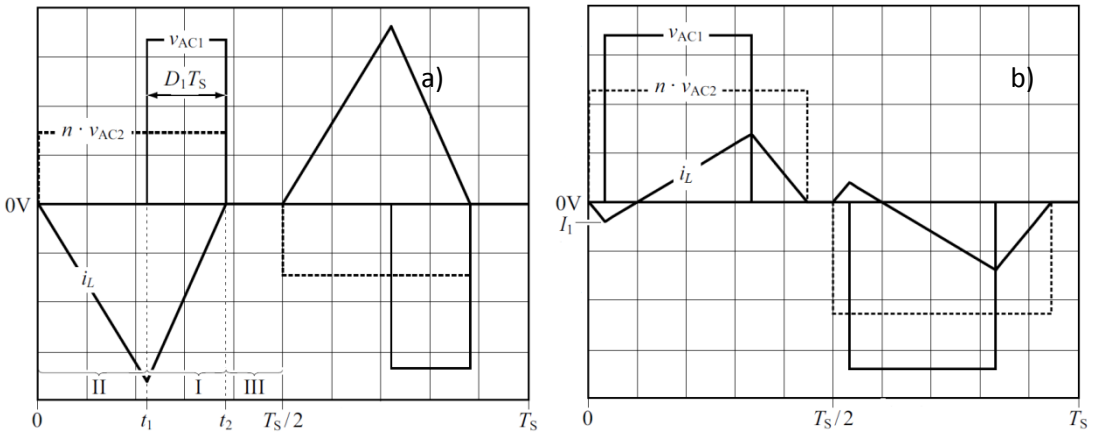


Fig. 20 *a) Transformer voltages and inductor current for triangular current mode modulation*
b) Modified triangular current mode modulation which enables HV side ZVS and LV side switching at zero transformer current.

Therefore, to obtain the low total switching losses, the modulation scheme needs to be modified, such that the LV side full bridge continues to switch at zero current and the HV side full bridge is operated with ZVS. The required modification to the modulation scheme introduces circulating transformer currents (*Fig. 20*. b), needed to achieve ZVS on the HV side. With this modified triangular modulation scheme, the maximum achieved power is far below the maximum possible power of the DAB.

Based on the lossless electric DAB model, the required duty cycles and the required phase shift angle are determined with:

$$D_1 = \frac{1}{\pi}\frac{nV_2}{V_1 - nV_2}|\varphi| + \frac{2f_S L(-I_0)}{V_1},$$

$$D_2 = \frac{1}{\pi}\frac{V_1}{V_1 - nV_2}|\varphi|,$$

$$\varphi = \frac{\pi f_S L I_0}{nV_1V_2}\left[V_1 - nV_2 - \sqrt{V_1(V_1 - nV_2)\left(1 + \frac{|P|}{f_S L I_0^2}\right)}\right]\mathrm{sgn}(P)$$

Typical efficiency values that can be obtained with this type of DC/DC converter are between 90% -95% and this is the greater since the ratio between the output voltage and the input voltage tends to the transformation ratio ***n***.

The project of the aforementioned DC/DC converter and its controller is complex and requires a more detailed discussion is beyond the above mentioned study. On the other hand there are today commercially available subsystems capable of providing the requirements summarized in the following table and employing the technologies described in this paragraph.

6 Charging unit

In order to achieve a high repetition accuracy, the capacitor bank has to be charged to the desired voltage with a high accuracy between two pulses. This task is performed by a charging unit which must ensure that the voltage drop of the capacitor bank is contained within less than *drop voltage specification*. The stored energy in solid state modulators generally is much bigger than the pulse energy.

In fact, the size of the capacitors bank is a function of the percentage voltage drop and the peak voltage. The charging unit must therefore, at start-up storing the energy necessary to achieve of the peak pulse voltage. Conversely, between each pulse will be required to integrate the energy transferred to the load, which is a negligible fraction of the total stored energy .

The size of the capacitor bank can therefore be a technological limit not easy to be solved. In fact, with the increase of the capacitive value grow the parasitic effects, which worsen the dynamic behavior. The main parasitic effects are manifest in the form of ohmic losses and reactive effects, due to the presence of leakage inductances.

While, the first type of effect it worsens the voltage drop with the increase of the current supplied from the capacitor, the second type of effect, in the presence of variation of the current, can give rise to oscillatory phenomena that can generate hazardous overshoot for semiconductor devices used as switches.
One way to overcome this obstacle is to resort to the simultaneous use of:

- Multicore transformer,
- Charging unit operating in interleaved mode.

The use of multicore transformer, in fact, allows to distribute of the energy, which overall must be accumulated by the sole bank of capacitors, in a number of capacitors equal to the number of cores from which the multicore transformer is constituted. Reduced size of the capacitors makes possible to use capacitors that have better dynamic performance.

Also, the total current required by the charging unit operating in interleaved mode will present a low ripple, it will result:

$$I_{rip} \propto \frac{1}{N^2}$$

where N is the number of the charging unit. In this way the dynamic performance requests to the preceding stage are less stringent and therefore the output capacitor of the last stage, which must be of a size comparable to the sum of the output capacitors of the individual charging units, may present less performing physical characteristics.
Another requirement to the charging unit is to increase the voltage level in order to ensure the pulse generator the correct voltage level to be modulated and converted by the pulse transformer.

6.1 DC/DC boost converter

Based on the requirements of the *charging unit*, the most suitable circuit appears to be that of the *DC/DC boost converter*. Moreover, to ensure a conversion efficiency comparable or superior to that of the remaining subsystems, since the output converter will raise the input voltage, it is possible to make operate this stage in *boundary conduction mode* (***BCM***) in other words the switching of the switches is occur at zero voltage (***Z**ero**V**oltage**S**witching*). This circuit solution allows to consistently reduce the switching losses, to reduce the size of the converter itself and simplifies the voltage balancing between the switches in series. In fact, the advantages and disadvantages between this operative mode and the *continuos conduction mode* (***CCM***) are summarized in the *Tab. 3*.

The boost converter is an electronic circuit device able to transfer energy at high level between the generator and the output load. This exchange of energy takes place through almost two reactive elements L_1 and C_{out}. The different energy level of the output is controlled by the charge and discharge of inductor that is connected in series with the output capacitor.
In order to explain the operation mode of the circuit converter (Fig. 21 a) is needed to divide the time in four interval considering that the operation is cyclic (Fig. 21 b). During the interval T_1 the switches are turned ON

and the input voltage V_{in} is applied to the inductor L_1. Therefore the inductor current i_L increases until the switches turn OFF. The inductor current reaches the level i_{Lp}[A2].

	Continuos Conduction Mode	Boundary Conduction Mode
Peak current: $I_{L,peak}$	1	≤2
RMS current: $I_{L,rms}$	1	≤0.57
AVG current: $I_{L,avg}$	1	≤0.5
Size Magnetics: $E = \frac{1}{2} L \cdot I_{L,peak}^{2}$	1	0.4
Power losses switch on: $P_{sw,on} = I_{L,avg}^{2} \cdot R_{sw,on} \cdot t_{on} \cdot f$	1	≤0.25
Power losses switch off: $P_{sw,off} = \frac{1}{2} C_{oss} \cdot V_{ds}^{2} \cdot f$	1	≤0.16
Common Mode noise: $I_{CM} = C_p \frac{d}{dt} V_{ds}$	0 dB	< -10dB

Tab. 3 ***Advantages and disadvantages between CCM and BCM***

In the first part of the interval T_2 the switches are turned OFF and the diodes are not conducting until the snubber capacitors does not start charging. In this case the inductor L_1 and the snubber capacitors C_S of the switches and diodes form a resonant circuit.

The inductor current i_L at this point (interval $T3$) will tend to decrease as the capacitors in parallel to the diodes and the output capacity tend to charge.

[A2] $\Delta i_{Lrise} = \frac{V_{in}}{L_1} T_1$, $\Delta i_{Lfall} = \frac{V_{in} - v_{out}}{L_1} T_3$

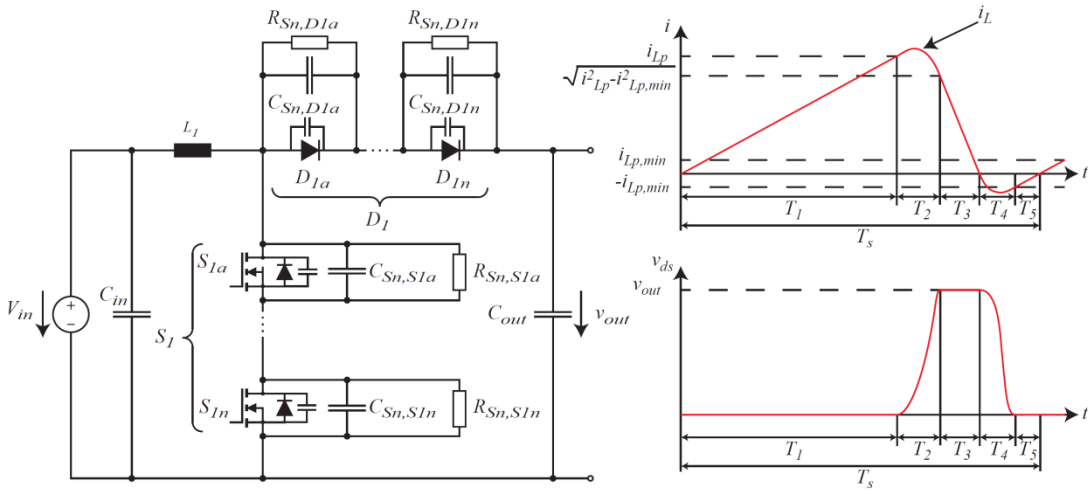


Fig. 21 *a) Boost converter scheme, b) waveform of the inductor current and the mosfet drain-source voltage.*

Obviously, while the maximum value of the positive voltage across the snubber capacitors will be limited by the conduction voltage of the diodes the voltage across the output capacitor will grow up to the value :

$$v_{out} = v_{in} + v_L = v_{in} + L_1 \frac{di_L}{dt} = v_{in} + L_1 \frac{\Delta i_{Lrise}}{T_3} \approx v_{in}\left(1 + \frac{T_1}{T_3}\right)$$

Since the T_3 interval can at most be less than or equal to T_1, the inductor current i_L at beginning of the interval T_4 will be zero (Zero Voltage Switching Boundary condition) if it is verified this relation $\Delta i_{Lrise} < \Delta i_{Lfall}$ that implies :

$$2\,V_{in} - v_{out} < 0 \qquad \text{Eq. 1}$$

In the interval T_4 again the inductor and the parasitic capacitors form a resonant circuit. During the time interval $T4$ the body diodes of the switches begin to conduct bringing quickly the switches in the conduction zone. In this way is concluded a whole controlled cycle of energy transfer.

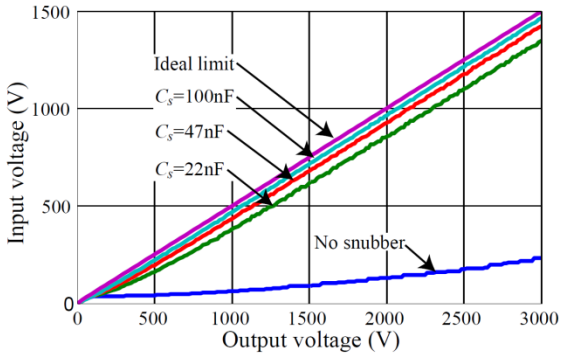


Fig. 22 *Upper limit for Vin to achieve ZVS for different snubber capacitance values per switch.*

The resonant transition during interval T_4 can be modeled as a resonant circuit with an equivalent capacitance of

$$C_{eq} = C_{Switch} + C_{Diode} \qquad \text{Eq. 2}$$

The input capacitor is modeled as a voltage source. At the beginning of the resonant transition, C_{eq} is charged to the output voltage and the inductor current is zero. With these initial conditions and assuming a linear capacitance, the circuit oscillates around the input voltage with an amplitude of

$v_{out} - V_{in}$. In a real system, the assumption of a linear equivalent parasitic capacitance is not entirely valid. The capacitances of the semiconductors show a strong voltage dependency. Because the capacitance increases significantly at lower voltages, more energy would be required to meet the ZVS condition.

However the influence of the non-linear capacitance of the semiconductors is reduced by the additional snubber capacitors. In *Fig. 22* is shown the upper limit of the V_{in} to achieve ZSV in function of the V_{out} and the snubber capacitors C_s.

Inside the ZVS operating area, a minimum inductor current is required to transmit power to the output. The minimum current for linear capacitances is:

$$i_{Lp,min} = \sqrt{\frac{C}{L}} \cdot \sqrt{(v_{out} - 2 \cdot v_{in}) \cdot v_{out}} \quad \text{[A3]}$$

where C is the equivalent capacitance during the resonant transition and L is the boost inductance. If the converter is operated below $i_{Lp,min}$ no power is transmitted to the output.

6.1.1 Series Connection of Switches

Since the system is operated at an output voltage of 3 kV, a series connection of several MOSFETs and diodes is required. To assure a balanced blocking voltage across the series connected devices, a snubber network, consisting of a parallel of resistor and capacitor, are added as shown in *Fig. 21* The resistor assures a static voltage balancing since the leakage current is in general not equal for all devices. The capacitors assure a balanced voltage across the switches during transients. These capacitors are required because the output capacitances are not equal and the MOSFETs do not switch at the same time instant due to jitter in the switching signals and component tolerances. The voltage difference of the blocking voltage after the turn off process can be described as follows:

$$\Delta V = \frac{i_0 \cdot \Delta T}{C}$$

where i_o denotes the current through the switches during the turn off process, ΔT is the jitter between the turn off signals and C is the snubber capacitance for assumption equal at each blocking voltage.

6.1.2 Converter Control

The controller that modulates the turn-on time interval can operate in one of two ways:

- by an on-time control,
- by a peak current control.

[A3] So that we can transfer energy from the inductor to the capacitor is necessary that current flowing into the capacitor C. This current must be equal to: $i_C = C\frac{\Delta V_o}{\Delta t}$ where it is: $\Delta V_o = v_{out} - 2V_{in}$.

The energy transferred to the capacitor will therefore equal to: $\Delta E = \frac{1}{2} i_C v_{out} \Delta t$ and it will have to match the decrease of energy in the inductor equal to: $\Delta E = \frac{1}{2} L \cdot {i_{Lp,min}}^2$. Therefore, by sharing the two equations and explaining everything in $i_{Lp,min}$ is obtained the above.

Both methods are mathematically equivalent. The peak current control additionally provides an over-current protection and is independent of the exact turn-on time of the switch.

The disadvantage of this control strategy is that the source current of the MOSFETs has to be measured. The on-time control requires only a zero-crossing detection of the inductor current in order to determine when the on-time starts.

In order to achieve a high repetition accuracy, a closed loop control is required. The feedback controller for the on-time control differs from the peak current control. The optimal time instance to turn on the switch is always at the end of T_4, regardless if ZVS is possible or not. This reduces the losses, since the conduction losses of the switch are lower than those of the internal body diode.

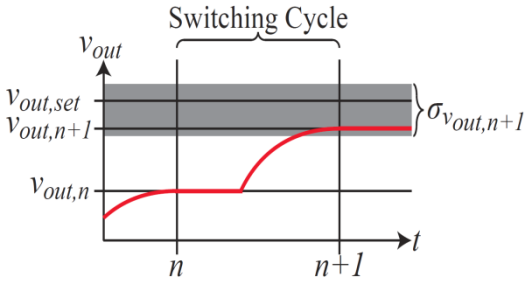


Fig. 23 *Sketch of the last switching cycle*

Since the converter is operated in BCM, the switching cycles are independent as the converter could stop operating at the end of each cycle. Hence, it is possible to use a ***cycle to cycle based feedback controller*** which calculates the required peak current i_{Lp} or the on-time T_{on} depending on the implemented converter control. Therefore the converter can be controlled by using an adaptive, time discrete controller. The change of the output voltage $v_{out,n+1} - v_{out,n}$ for a capacitive load within one switching cycle is:

$$v_{out,n+1} - v_{out,n} = \sqrt{a} + V_{in} - v_{out,n} \quad \text{[A4]}$$

with:

$$a = Z^2(i_{Lp}^2 - i_{Lp,min}^2) + (V_{in} - v_{out,n})^2,\ Z = \sqrt{\frac{L_1}{C_{out}}}$$

The required ***peak switch current*** can be calculated by using previous reports with $v_{out,n+1} = v_{out,set}$:

$$i_{Lp} = \sqrt{\frac{C}{L} \cdot \alpha + \frac{C_{load}}{L} \cdot \beta}$$

[A4] It is possible to evaluate this relationship, starting from the following equations:

$$\frac{1}{2} L \cdot {i_{Lp}}^2 = \frac{1}{2} C \cdot \left(v_{out,n+1} - 2 \cdot V_{in}\right) \cdot v_{out,n+1}$$

$$\frac{1}{2} L \cdot {i_{Lp,min}}^2 = \frac{1}{2} C \cdot \left(v_{out,n} - 2 \cdot V_{in}\right) \cdot v_{out,n}$$

subtracting both members of the two equations and rewriting everything according to the following amount:

$$v_{out,n+1} - V_{in}$$

it will arrive :

$$\frac{L}{C} \cdot \left({i_{Lp}}^2 - {i_{Lp,min}}^2\right) + \left(V_{in} - v_{out,n}\right)^2 = \left(v_{out,n} - V_{in}\right)^2$$

with :

$$\begin{aligned}
\alpha &= \begin{cases} (v_{out,n} - 2V_{in})v_{out,n} & v_{out} \geq 2V_{in} \\ 0 & v_{out} < 2V_{in} \end{cases} \\
\beta_1 &= v_{out,set} + v_{out,n} - 2V_{in} \\
\beta_2 &= v_{out,set} - v_{out,n} \\
\beta &= \begin{cases} \beta_1 \cdot \beta_2 & v_{out,n} < v_{out,set} \\ 0 & v_{out,n} > v_{out,set} \end{cases}
\end{aligned}$$

For an ***on-time control based*** controller, the on-time can be calculated with:

$$T_{on} = \frac{L}{V_{in}} \cdot i_{Lp} = \frac{L}{V_{in}} \cdot \sqrt{\frac{C}{L} \cdot \alpha + \frac{C_{load}}{L} \cdot \beta}$$

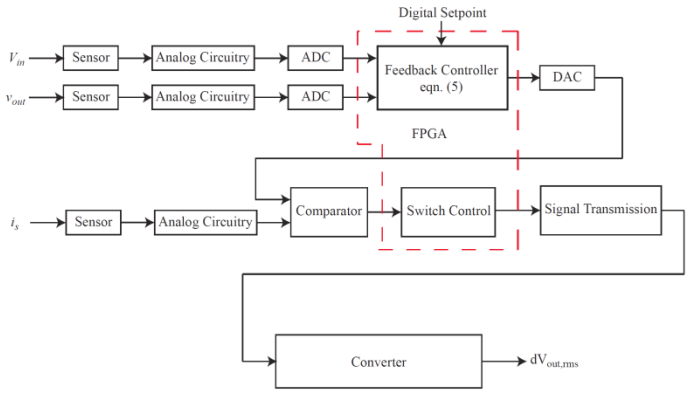


Fig. 24 *Schematic of the control hardware.*

A schematic of the control hardware is shown in *Fig. 24*. The control hardware incorporates three measurement inputs: the converter input voltage, the output voltage and the switch current. The voltages are measured by using an RC voltage divider. The source current of the MOSFETs is measured with a shunt. The measured signals are fed via a pre-amplifier stage to the ADC inputs and the comparator input respectively.

The input and output voltage are sampled by an ADC which is connected to an FPGA. The feedback controller output is converted to an analog output signal by an DAC. This signal is then compared with the measured switch current in order to determine when the switches have to be turned off for a peak current controlled system.

The switch control implemented in the FPGA generates the switching signal depending on the operating conditions. Finally, the switching signal is converted into an optical signal which is transmitted to the converter. The design of the converter controller, implies to control the behavior of the charging unit at an impulsive change in load. In other words for the design of controllers it needs to dimension the parameters (parasitic resistance of the capacitor ESR) that influence the output dynamic impedance.

7 Pulse generator

In an pulse modulator, the electronic stage that is technologically more complex to be designed and implemented is the pulse generator. This stage can be decomposed into the following subsystems:

- commutation Switch,
- Pre-magnetising circuit,
- Pulse transformer,
- possible L-C Bouncer,

interconnected according to the layout shown in Fig. 25.

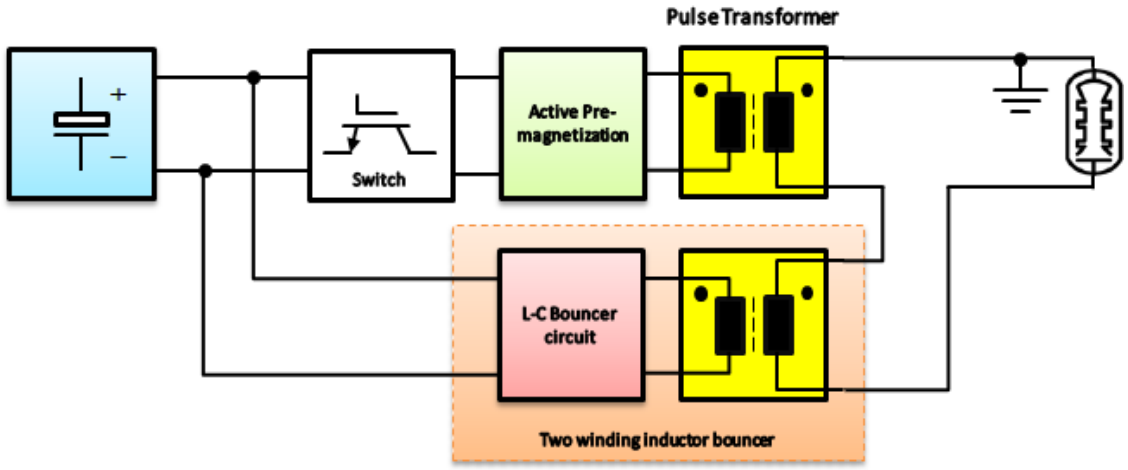


Fig. 25 *Typical layout of the Pulse generator*

Before proceeding with the detailed description of each subsystem it is necessary to contextualize the overall layout to the case under study. Therefore is necessary to briefly summarize the project parameters that constrain the design/implementation and these are:

- the maximum peak voltage to the modulator output,
- the maximum rise time, overshoot and drop voltage of the step response,
- the maximum energy transferred per pulse.

It will start by evaluating the effect of accumulated energy and transferring from the modulator, in fact the energy transferred to the load at each pulse is a small fraction of the energy that is needed to store to obtain the preset value of the flattop voltage.

This consideration therefore obliges the designer to evaluate all the circuit solutions that allow to accumulate large electrostatic energies and to release them small quickly (capacitors with low ESR, capacitors with a high density of storage energy).

The first solution, that can be used, is distribute the electrostatic energy to be storage with multiple charging units connected to the same bank of input capacitor. Additionally, using an interleaved mode control of

charging units during the period when the output voltage to the modulator is null, it is possible to assure a low distorted current demand at the previous stage.

The second solution, which integrates with the first one, is to convey the electrostatic energy, previously fractionated, to the load and simultaneously raising the value of the flattop voltage. To this purpose, the pulse transformer used to increase the output voltage is made by several ferromagnetic cores. In this way, using a single secondary winding that concatenates the magnetic flux of individual cores, it is possible to obtain a high output voltage without having to resort to a high number of secondary coils (reduced the output distributed capacity) and to ensure the required energy transfer.

Therefore in this way it is possible to use a further parameter in the design phase to observe the constraint on the output voltage at the flattop and the pulse rising time.

Precisely in this circumstance, the relationship of the transformation ratio, besides, depend on the turns ratio will also depend on the relationship between the concatenated magnetic flux. In fact, unlike a normal transformer where the concatenated primary flux is practically equal to the concatenated flux to the secondary, in a multicore transformer, the secondary flow may be higher than the primary flow or vice versa. Thus indicating with A_1 the average area enclosed by the primary spirals and with A_2 the mean area enclosed by the secondary spins will result :

$$\frac{V_2}{V_1} = n_{coil,leg} \cdot \frac{A_2}{A_1}$$

where it is :

$$n_{core} = \frac{A_2}{A_1} \qquad\qquad n_{coil,leg} = \frac{N_2}{N_1}$$

This solution by acting on the number n_{core} of the magnetic core allows to contain the number of turns of the secondary winding and improve the rise time that depends on the square of the latter.

Another resulting advantage is a reduction in magnetic and electrostatic energy accumulated between the primary and secondary winding with respect to the case where the secondary windings are connected in series.

In fact, in the example shown in Fig. 26, with the same total magnetic flux and in compliance with the safety distances[A5] between primary and secondary windings, it is possible to see the difference of dimensions (hatched areas) between a solution in which has a number of secondary windings connected in series equal to

[A5] The safety distance $d_{w,min}$ between primary and secondary winding depends by the E_{peak} maximal tolerable peak electic field in oil (*20kV/mm* for short pulses of few microseconds), r_r the inner radius of the cylinder (guard ring) and v_s the secondary voltage, according to the following relationship:

$$d_{w,\min} = r_r \exp\left(\frac{v_s}{r_r E_{\text{peak}}}\right)$$

the number of magnetic cores and that in which is present a solution with only two secondary windings each spanning all the magnetic cores.

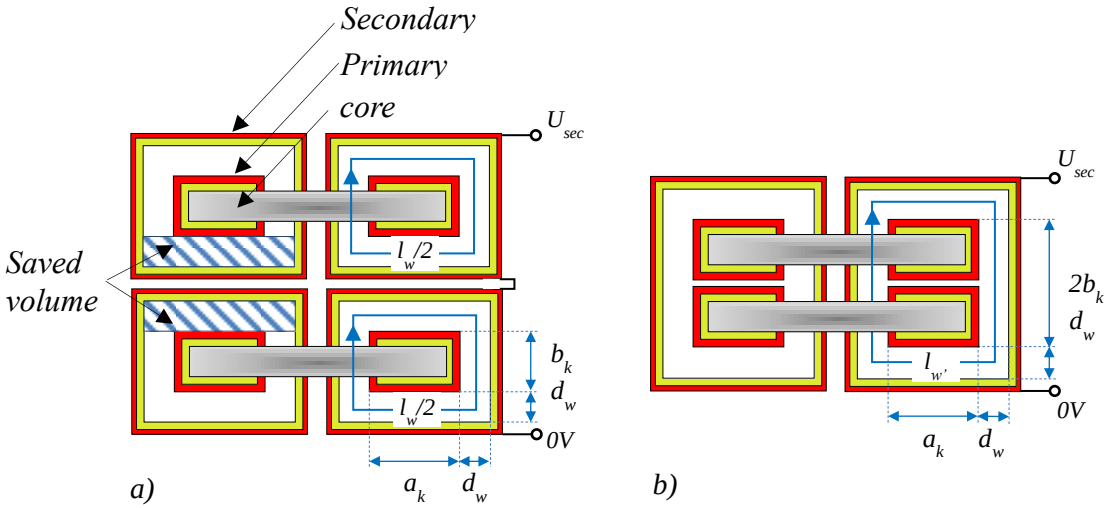


Fig. 26 *Saved volume between the primary and secondary windings, resulting in a reduced leakage inductance when using (b) the matrix transformer, instead of (a) a transformer series connection.*

In general, this transformer configuration is called the multicore-transformer [5]. This type of transformer for its peculiarities must be made with primary windings at a reduced number of turns. In fact we shall see in the following paragraphs that with the increase of the number of cores decreases the magnetic flux density for the core, and then the number of primary winding turns.

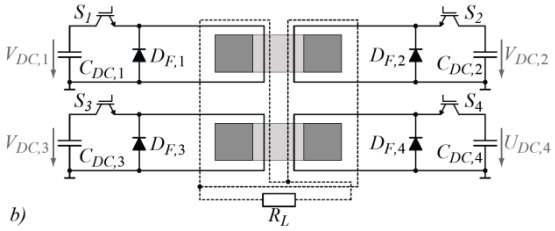


Fig. 27 *Schematic of the solid-state modulator with two cores, two primary windings arond each core, and secondary enclosing both cores.*

Furthermore, in the case of medium-large energy transfers per pulse, to optimize the value of ampere-turn per core, it is preferred to use a solution with two switches per core (see *Fig. 28*) to halve the current handled by each switch and halve the energy managed by each Charging unit stage.

If the pulse duration is short (μs order), since that the pulse energy transfer is low, to reduce the flux leakage at the primary, a double primary winding connected in parallel is used. In fact, it must remember that, how much less is long the time rise of the magnetomotive force as much less the magnetic flux penetrates the center of the core (magnetic skin depth) and therefore the greater is the magnetic reluctance of the core. This effect involves the re-closing of the flow along the external lines at the magnetic core and thus a leakage inductance increase. Therefore, to counteract this increase of the leakage inductance and of the magnetizing current is used a redistribution of the magnetomotive force for each transformer leg.

In summary, the primary winding of the multicore-transformer is made with a few coils, (ribbon type or conductive film type) wrapped around each leg of the magnetic core and connected in parallel at only one switch per core.

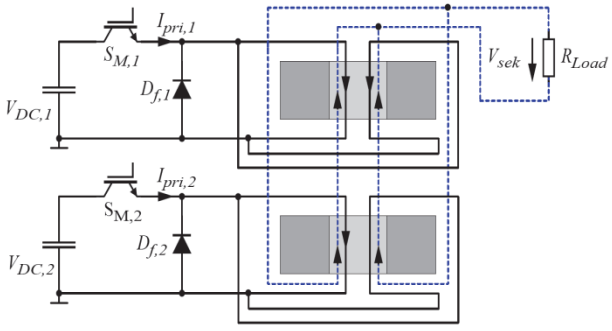


Fig. 28 *Schematic of the solid-state modulator with two cores, two primary windings around each core fed in parallel from a single switch per core, and secondary enclosing both cores*

The secondary winding in a similar fashion will consist of only two windings connected in parallel, opportunely isolated from the individual primary windings, arranged so as to embrace each half of the legs from which is composed the multicore-transformer.

In *Fig. 28* is shown, by way of example, the construction of a multicore-transformer consisting of only two magnetic cores.

This solution allows, by comparison, a reduction of the:

- overall volume,
- number of winding turns,
- flux leakage,
- electrostatic energy stored between primary and secondary windings.

In other words, this solution will reduce the leakage inductance $L_{\sigma 1}, L_{\sigma 2}$ and the distributed capacitance C_d, which depend on:

$$L_{\sigma 1} \propto {N_1}^2 \cdot V_{12} \qquad L_{\sigma 2} \propto {N_2}^2 \cdot V_{12}$$

$$C_d \propto \left(\frac{N_2}{N_1}\right)^2 \cdot V_{12}$$

where N_1 , N_2 are the winding turns and V_{12} is the volume between the windings.

Another problem, that occurs only in the HV pulse transformers due to the constraint on the *interlaminar voltage* is the necessary oversizing of the magnetic-core cross-section. In fact, if the pulse energy transferred from the transformer to the load is low, the dynamic of the flux swing is small and thus also the cross-section required.

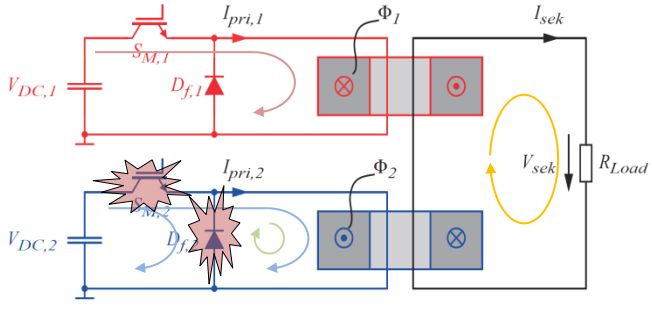


Fig. 29 *Condition of stress due to a non-synchronous switching*

However, for assigned magnetic tape with which the core is made, if the interlaminar voltage is higher than the maximum permissible voltage, the designer is forced to oversize the magnetic core, so as to increase the number of sheets per cross section[A6].

Whatever the solution used to feed the multicore-transformer, in order to reduce the

[A6] To reduce the interlaminar voltage, it is possible:
- reduce the voltage on the primary windings by increasing the number of magnetic cores,
- increase the interlaminar dielectric resistance,
- dividing the cross section of the core.

switching losses is important to synchronize opportunely the switches using to an active gate control.
In fact, a possible delay of the switch $S_{M,2}$ respect at the $S_{M,1}$, results in the creation of an induced current in the primary winding (green trace), which circulates in the freewheeling diode $D_{f,2}$. When the $S_{M,2}$ switch is in "on" state, the $D_{f,2}$ diode will continue to be crossed by current, even though it is inversely polarized, due to the release time of the accumulated minority charges near the emptying region. In this case, to balance the current on the second primary winding, it is necessary to compensate the spilled current by the diode by increasing the current supplied by the switch. Therefore, this operating condition creates a stress for both the freewheeling diode that for the switch (see *Fig. 29*).
The active gate control will allow to monitor the voltage and the current in the switching phase, so as to schedule the gate signal of the switches and to avoid a hard commutation of the freewheeling diode and protecting the modulator from a potentially dangerous overcurrent to the load (arc current monitor).
In the paragraphs that follow describe in detail the technological solutions adopted for each of the subsystems shown in *Fig. 25*, focusing on the design criteria to be adopted in order to realize a pulse transformer to work with secondary voltages next to a million volts.

7.1 Switches and driver circuits in the pulse generator

The primary winding voltage modulation is obtained by semiconductor devices such as IGBTs (Insulated Gate Bipolar Transistor), which unlike the other semiconductor devices show a good compromise between the voltage/current switching and the maximum switching frequency. However, the IGBTs have advantages and disadvantages. The disadvantages of these devices are the lower blocking voltage and lower current rating compared with spark gaps. Therefore, multiple semiconductor switches have to be connected in series and/or in parallel. To reduce the number of required switches, they have to be operated at the highest current as possible.
The efficiency of a pulse generator, from the point view of the switching devices, depends on the ***conduction losses*** and the ***switching losses*** of the IGBT. While the first depend essentially on the constructive physical characteristics of the device, the latter depend on the driver circuit.
IGBT Conduction losses can be calculated using an IGBT approximation with a series connection of DC voltage source (v_{CE0}) representing IGBT on-state zero-current collector-emitter voltage and a collector-emitter on-state resistance (r_C):

$$v_{CE}(i_C) = v_{CEO} + r_C \cdot i_C$$

The same approximation can be used for the anti-parallel diode, giving:

$$v_{D0}(i_D) = v_{DO} + r_{D0} \cdot i_D$$

These important parameters can be read directly from the IGBT Datasheet (cf. *Fig. 30*) and increasing these to a safety factor that is typically between 1.1. and 1.2 .

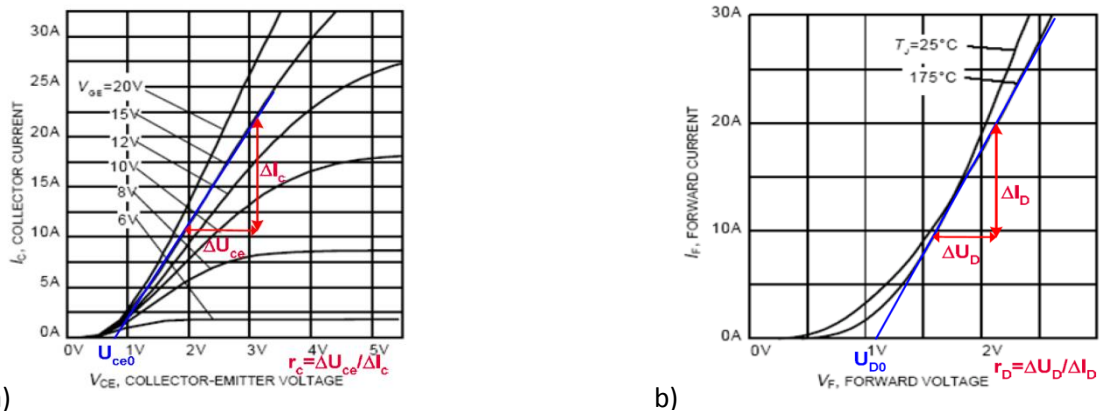


Fig. 30 *a) Typical output characteristic of IGBT and* $\boldsymbol{r_C}$, $\boldsymbol{v_{CE0}}$ *estimation*
b)typical diode forward current as a function of forward voltage and $\boldsymbol{r_D}$, $\boldsymbol{v_{D0}}$ *estimation.*

The instantaneous value of the IGBT conduction losses is:

$$p_{CT}(t) = v_{CE}(t) \cdot i_C(t) = v_{CE0} \cdot i_C(t) + r_C \cdot i_C^2(t)$$

If the average IGBT current value is I_{cav}, and the rms value of IGBT current is I_{crms}, then the average losses can be expressed as:

$$P_{CT} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{CT}(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (v_{CE0} \cdot i_C(t) + r_C \cdot i_C^2(t))dt = v_{CE0} \cdot I_{Cav} + r_C \cdot I_{Crms}^2$$

The instantaneous value of the diode conduction losses is:

$$p_{CD}(t) = v_D(t) \cdot i_D(t) = v_{D0} \cdot i_D(t) + r_D \cdot i_D^2(t)$$

If the average diode current is I_{Dav}, and the rms diode current is I_{Drms}, the average diode conduction losses across the switching period (T_{sw}=$1/f_{sw}$) are:

$$P_{CD} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{CD}(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (v_{D0} \cdot i_D(t) + r_D \cdot i_D^2(t))dt = v_{D0} \cdot I_{Dav} + r_D \cdot I_{Drms}^2$$

Therefore, in the design phase, the IGBT device has to be chosen, for given pulse current, with lower collector-emitter on-state resistance. If there was not a single device able to switch the required current, it should to employ a parallel combination of them. Same consideration should be made for the freewheeling diode.

7.2 IGBT Driver

The control circuit of an IGBT as already anticipated conditions the efficiency of the pulse generator, (it allows to contain the switching losses and avoid the hard commutation due at non synchronous switching for

circuital asymmetries or for physical characteristics of the switch out of tolerance), but constitutes an essential element in the fault management of the modulator (short circuit protection, overvoltage protection). There are several possible circuit solutions developed by the power electronics industry, however, today, the most circuit used commercially is based on voltage source driver (cf. ***Fig. 31*** a).

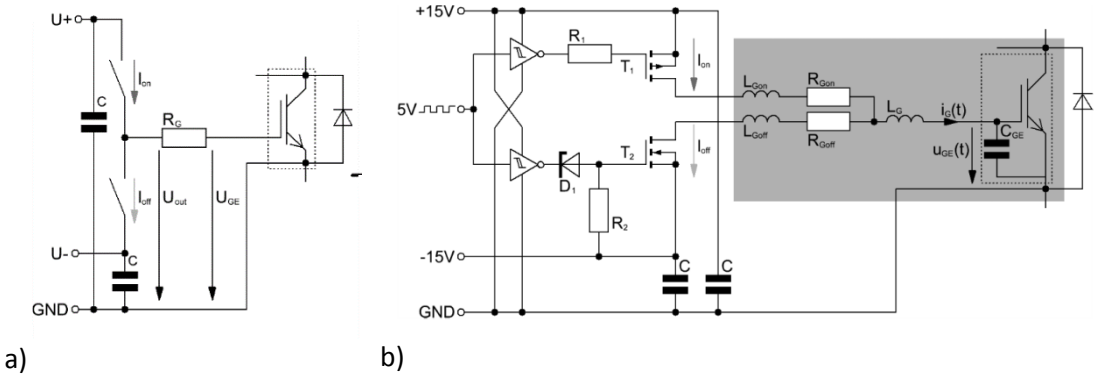


Fig. 31 *a)Basic circuit of a voltage source driver b)driver stage with parasitic elements*

The gate drive, to reduce the switching losses will have to ensure fast switching transients, in both opening and closing of the switches or will have to show a resistance and a parasitic inductance and capacity as low as possible.

In fact, the equivalent model of an IGBT has a parasitic capacity and inductance (cf. shaded area in *Fig. 31* b) that, together with the resistance and inductance of the gate drive, can change the pulse response of the device. In an IGBT the parasitic capacitance of the gate C_{GE} is not constant with the variation of the gate voltage v_{GE}. Moreover, in an IGBT, the typical relationship between voltage v_{GE} and charge accumulated in the gate-emitter region is reported in *Fig. 32*. This response curve allows to evaluate the trend of the parasitic capacitance C_{GE} as a function of voltage v_{GE}.

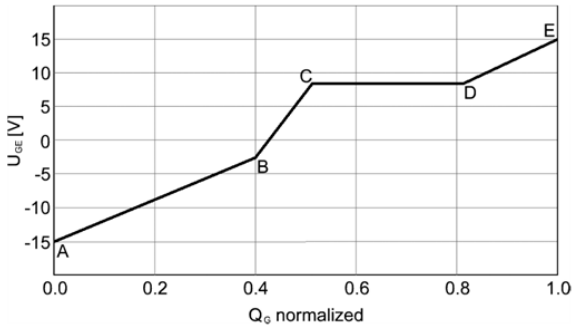


Fig. 32 *Gate voltage v_{GE} in dependency of the normalised IGBT gate charge Q_G*

In this regard in *Fig. 32* it is possible to identify four different operating zones. The area identified by the points B and C is the area in which the conduction threshold voltage of the IGBT exceeds and it is characterized by a value of the C_{GE} capacity in absolute lowest.

The next zone (betwen the points C and D) is observed a growth of gate charge without any change of the voltage v_{GE} because this is accumulated in the depletion region of the collector-gate. This zone is called the "Miller

voltage" region because the increase of the gate capacitance is manifested due to the Miller effect (equivalent capacitance of the gate-collector C_{GC} reported to the gate-emitter junction).

In full saturation of the IGBT ($V_{CE} = V_{CEsat}$), the charge Q_G accumulated in the gate-emitter region begins again to rise with increasing v_{GE} voltage. Therefore, the gate capacity continue to rise but with a lower rate because the C_{GC} contribution decrease for the Miller effect (the IGBT gain goes down).

Therefore, the gate capacitance C_G of the IGBT, in deep switching, assumes its maximum value thus making the longer the switch-off transient.

Based on the considerations made, the gate drive circuit must provide a:

- fast turn on of IGBT : by the use of a ***double stage turn on*** as the *gate boosting circuit,*
- fast tun off of IGBT : by the use of a ***double stage turn off*** and a v_{CE} voltage clamping.

Moreover the gate drive must provide a fast detection system (short-circuit detection) of the over current and the over di/dt by the use of a Rogowski coil.

7.2.1 Double stage turn on

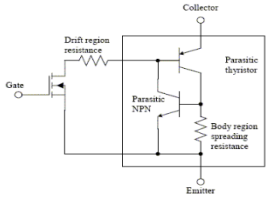
To achieve a fast turn-on, a high gate-emitter voltage $\boldsymbol{v_{GE}}$ is required. A high $\boldsymbol{v_{GE}}$ results also in a high maximum collector current $\boldsymbol{i_c}$, which could lead to a latchup or high thermal stress during a short-circuit event. Hence, the $\boldsymbol{v_{GE}}$ has to be set such that a safe operation is guaranteed or it has to be reduced after the switch is turned on.

This technique is known as gate boosting [7] and consist in to impose a voltage at the gate of the IGBT higher than the threshold voltage $\boldsymbol{v_{GE}}_{(TO)}$ at the beginning of the turn-on process and then reduce this as soon as the collector voltage $\boldsymbol{v_{CE}}$ of the IGBT reaches a predetermined value or after a predetermined time interval (about 1 µs).

In this way choosing a gate impedance R_G as small as possible ensures a large gate current that accelerates the switching process in the initial phase by reducing switching losses. However to ensure a soft interdiction of the freewheeling diode, the charging process of the gate capacitance must be done slowly after reaching the threshold voltage of the IGBT, by resorting to a reduction of the gate voltage and an increase of the resistance of the driving circuit. This operating mode therefore allows to reduce the switching losses without damaging the diode.

The R_G resistance of the driving circuit in the design phase will be dimensioned according to the maximum peak current I_{peak} in order to avoid the IGBT's static latchup (inability to switch off the device through only the gate control [A7]).

[A7] The parasitic NPN transistor of the IGBT as a result of the current outside the operating range gives rise to a thermal deriving of the static gain of the transistor which will bring it into saturation thus rendering the device insensitive to any gate control.



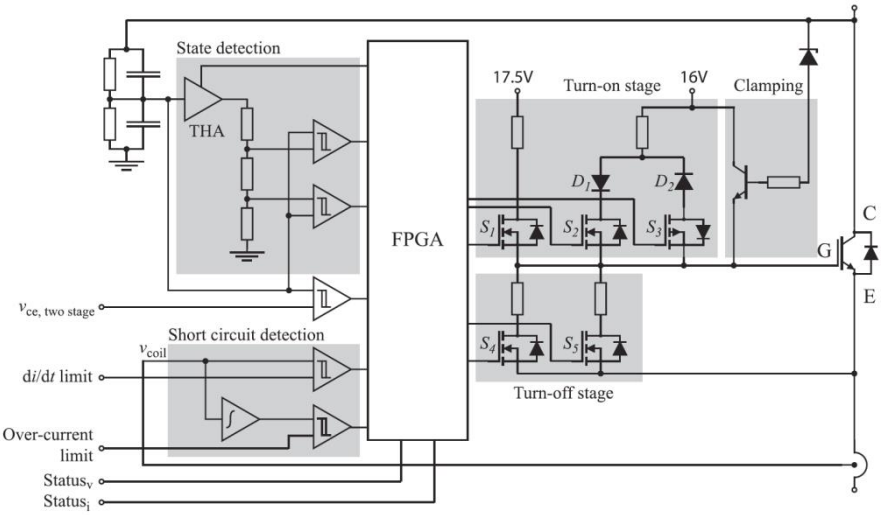


Fig. 33 *Example structure of the driver gate unit.*

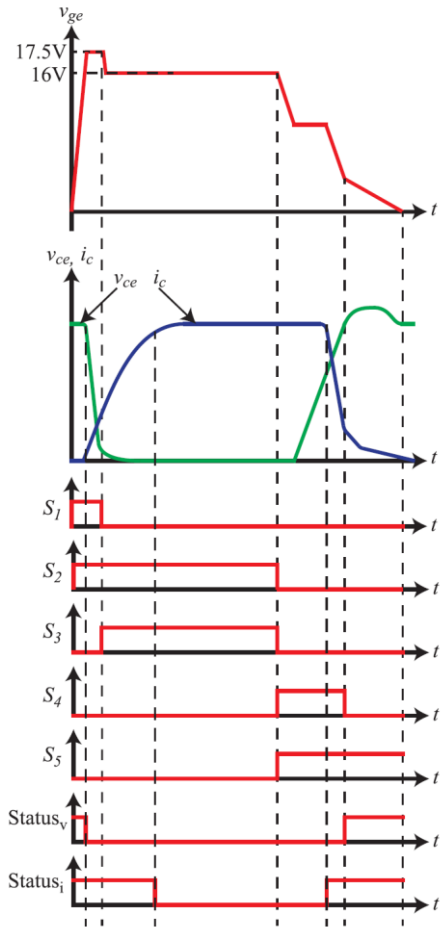


Fig. 34 *Gate-emitter voltage,* $\boldsymbol{v_{ce}}$ *and* $\boldsymbol{i_c}$ *and signals for* $\boldsymbol{S_1}$ *to* $\boldsymbol{S_5}$ *and status signals for one switching cycle during the normal operation.*

$$I_{peak} = \frac{2}{e} \cdot \frac{\Delta U_{GE}}{R_{G,min}} \approx 0.74 \cdot \frac{\Delta U_{GE}}{R_{G,min}}$$

However, if it is not possible to reduce the inductance of the driving circuit is necessary to increase the gate resistance previously calculated to prevent the IGBT control voltage and thus the collector current result oscillating and potentially dangerous for the freewheeling diode.

In fact, remember that the condition to be met, so that the free response of the control circuit do not result oscillating, is the following:

$$R_{G,min} \geq 2\sqrt{\frac{\Sigma L_G}{C_{GE}}}$$

ΣL_G: Sum of the gate lead inductances ($L_G + L_{Gon}$ or $L_G + L_{Goff}$) [H]

Therefore, the gate boosting technique is realized with two voltage sources with different levels. These two sources are connected in different moments through the switch S_1, S_2 and S_3 that are controlled by a specifically programmed FPGA.

Indeed, the latter to make fast the IGBT switching, after a predetermined time interval (about 1 μs) or when the $\boldsymbol{v_{CE}}$ voltage reaches a predetermined fraction of the measured value and maintained at the beginning of the turn-on process, will reduce the $\boldsymbol{v_{GE}}$ of gate voltage.

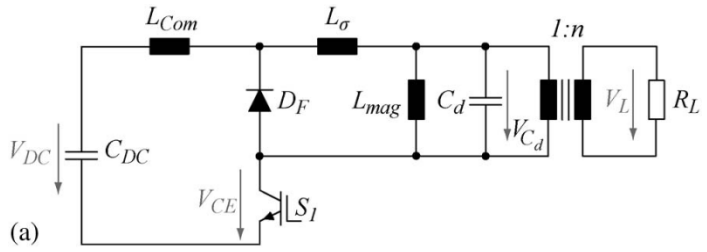
In other words, at the beginning of turn-on process, a track and hold amplifier (THA) will keep the value reached by the voltage $\boldsymbol{v_{CE}}$, also, the switches S_1 and S_2 will be closed while the remaining will be open (see *Fig. 33*).

The gate voltage of the IGBT, therefore, will begin to grow rapidly, since the gate impedance is the parallel of the impedances of the two voltage sources. When the gate voltage exceeds 16V the impedance of the gate increases (the diode D_1 is turns off) thus reducing the falling down speed of the voltage $\boldsymbol{v_{CE}}$.

As soon as this voltage is below a fraction of the measured voltage collector at the beginning of the turn-on process, or, after a predetermined time interval, it opens the switch S_1 and closes the switch S_3 which will lower the voltage gate by flushing the gate-collector junction. The turn-on process will end with the opening of the switch S_1 and S_5.

7.2.2 Double stage turn off and voltage clamping

To reduce the switching losses during the turn-off process is necessary to minimize the time in which the IGBT remains shorted. The maximum switching speed during the turn-off is basically limited by the overvoltage during the turn-off caused by the leakage inductance in the current commutation path. In fact, at turn-off a high switching speed with high dv_{ce}/dt and high di_c/dt would result in large over-voltages v_{ov} due to the parasitic inductance L_{Com} of the commutation path (e.g. L_{Com} = 40 nH and $di/dt \approx$ 5000 A/μs the overvoltage at turnoff is approximately 200 V).



$$v_{ov} = L_{Com}\frac{di_C}{dt}$$

Fig. 35 *Equivalent circuit of the pulse generator with the pulse transformer and typical overvoltage on the IGBT collector due to* L_{Com}

However, the total inductance along the commutation path can be modified by the system designer only within certain limits by appropriately selecting the critical components (parasitic inductance of the capacitor C_{DC}) and the PCB layout (cf. *Fig. 35*). The smaller value of this inductance is typically less than hundred nano Henry.

Suppose now that it is not possible to reduce the parasitic inductance, to have a high-switching speed and limit the overvoltage between the emitter-collector junction of the IGBT can be employed a drive circuit of

type ***zener clamping***. This circuit, in fact, bypass the IGBT soon as it exceeds the zener voltage. The zener current in correspondence to exceeding the Zener voltage is set by a resistor R_{fb} series of feedback (cf. *Fig. 36*a).

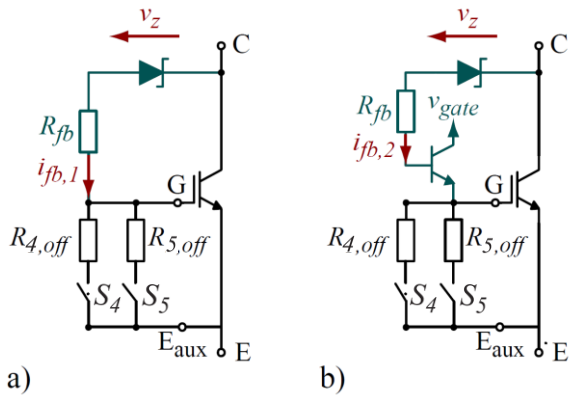


Fig. 36 *Implementation of a) the conventional zener clamping circuit and b) the improved zener clamping circuit.*

This configuration very similar to bootstrapping, as well as limiting the overload voltage, reduces the dynamic capacity of the IGBT gate-collector that allows faster switching times.

To reduce the power losses associated with the Zener current is possible to employ a configuration that use an NPN transistor along the feedback chain (cf. *Fig. 36*b). In this way improves the efficiency of the pulse generator as the pulse repetition frequency increases.

Furthermore, the current slope di_c/dt or the voltage slope dv_{CE}/dt depend by the gate resistor R_{off} and by the gate capacitors C_{GE}, C_{GC} (cf. *Fig. 37*), where the latter are dependent on the voltage v_{GE} and v_{CE} (see previous paragraph).

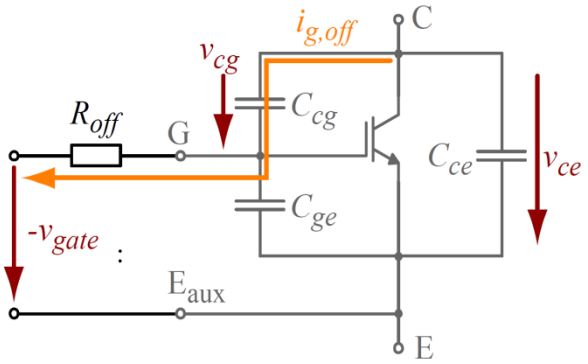


Fig. 37 *Influence of the gate resistor R_{off} on the current and voltage slope* di_c/dt *respectively* dv_{CE}/dt.

To avoid the limitation of the di_c/dt, and to reduce the turn off losses it is possible to use a ***double-stage drivers*** for IGBT modules. The double-stage driver consists of a low and high resistive turn-off stage splitting the switching operation in two different switching sections, for controlling the rate of gate discharge or the dv_{CE}/dt depending on the IGBT voltage v_{CE} as depicted in *Fig. 38*.

In the first section, during T_1, both stages S_4 and S_5 are turned on and the IGBT voltage v_{ce} is below the reference voltage v_{ref} . The IGBT gate is quickly discharged on a resistor $R_{off,4}||R_{off,5}$ to achieve a short turn off time and small switching losses. As soon as the IGBT voltage v_{ce} exceeds the specified voltage level v_{ref} at T_1, the low-resistance stage S_4 is turned off and the gate will be discharged through the high-resistance stage S_5 with $R_{off,5}$ during T_2. Due to the Miller capacitance, the change of the gate resistor from $R_{off,4}||R_{off,5}$ to $R_{off,5}$ results in a decreased current/voltage slope (cf. *Fig. 38*b).

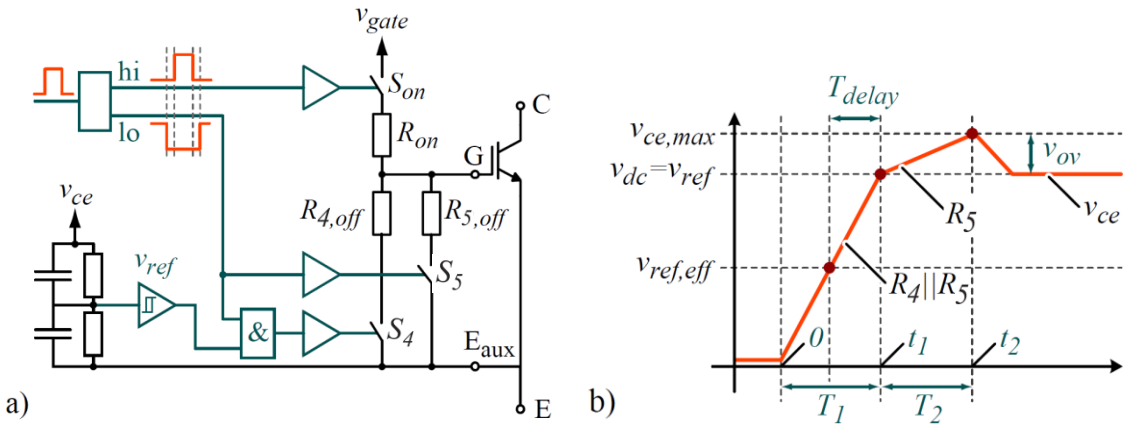


Fig. 38 *a) Block diagram of the double stage driver circuit and b) resulting voltage and current waveform of vce and ic during double-stage turn off.*

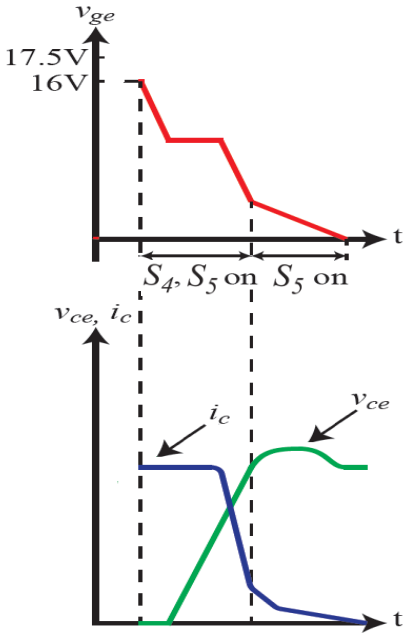


Fig. 39 *Resulting voltage and current waveform of v_{be}, v_{ce} and i_c during double-stage turn off.*

In order to reduce the switching losses the reference voltage v_{ref} is set to a value close to the dc-link voltage v_{dc} so that the parasitic inductance voltage is tolerated dall'IGBT and v_{ce} voltage drops as quickly as possible in the interval time in which the current is large (cfg.*Fig. 38*b and *Fig. 39*).

Due to the delays in the comparator and driver circuit (T_{delay}), the effective reference voltage $v_{ref,eff}$ has to be set below the dclink voltage v_{dc} to achieve a change of the gate resistor at v_{ce} $\approx v_{dc}$. To minimize this effect, the signal delay T_{delay} has to be minimized to guarantee a stable performance for various operating conditions (typical value $T_{delay}\approx$40ns).

The IGBT voltage v_{ce} is monitored with a balanced ohmic-capacitive voltage divider, where the overstepping of the reference voltage v_{ref} is detected with a high speed comparator (cf. *Fig. 38*a).

7.2.3 Short-Circuit Detection

To react as fast as possible on short circuits during the turn-on process, an over-di/dt detection is used. For this purpose can be used a PCB Rogowski coil. Since the Rogowski coil provides an output voltage proportional to the di/dt, the coil signal can be directly used for over-di/dt detection furthermore the coil voltage can be used to measure the collector current. Due to the operating principle of the Rogowski coil, the voltage $\boldsymbol{v_{Coil}}$ must be integrated in order to obtain the IGBT current. For relatively large mutual inductances M the integration can be done passively with a simple RC-low-pass filter. There, the cut-off frequency of the

filter defines the lower frequency limit of the current measurement. For achieving a small measurement bandwidth a low cut-off frequency of the RC-filter is necessary. The low cut-off frequency, however, leads to a high attenuation of the current measurement signal at higher frequencies. In case of small mutual inductances, i.e. small measurement signal amplitudes, this would lead to a low signal quality. Therefore, the signal has to be integrated actively for smaller mutual inductances. Basically, also a combination of passive and active integration is possible. The integrated voltage, which is proportional to the current, is fed to comparator K_1 (cf. *Fig. 40*) in order to detect the rising and falling edges of the pulse current. With comparator K_2 an over current can be detected and the IGBTs can directly be turned off very fast via the FPGA in order to protect the modulator. The peak values of the IGBT currents are detected and sampled by the ADC, which can be integrated in a DSP.

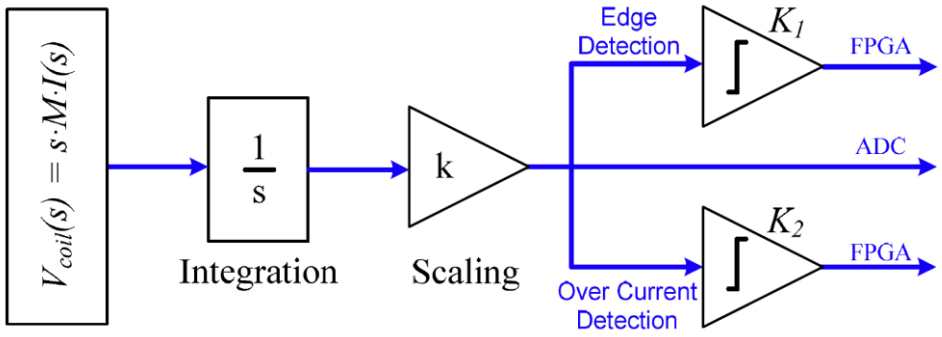


Fig. 40 *Block schematic of the measurement and signal processing electronic with edge detection K_1, over current shutdown and peak value measurement K_2*

Two comparators are used to detect short circuits (cfg. *Fig. 33*). As soon as the measured current exceeds a certain limit imposed on the comparator, the gate unit detects the short circuit. The first comparator is used to detect an over-di/dt, the second detects an overcurrent. As soon as a short circuit is detected, the short circuit turn-off procedure is initiated.

When the gate unit detects a short circuit, the switch is turned off immediately. At the beginning, the turn-off procedure is the same as during the normal operation. Since $\boldsymbol{v_{CE}}$ rises much faster than during the normal turn-off (due to the high current $\boldsymbol{i_c}$), the propagation delay of the normal two-stage turn-off circuitry is too high.

Therefore there are two different control modes:

- ***Short-circuit time controlled***,
- ***Short-circuit v_{CE} controlled***.

In the first mode both the two switches S_4 and S_5 remain turned on during the entire turn-off process which will end after a delay time T_{delay} from the instant in which the comparator reveals the exceeding of predetermined reference threshold. Therefore, at the end of the cycle we will have the simultaneous opening of the two switches S_4 and S_5.

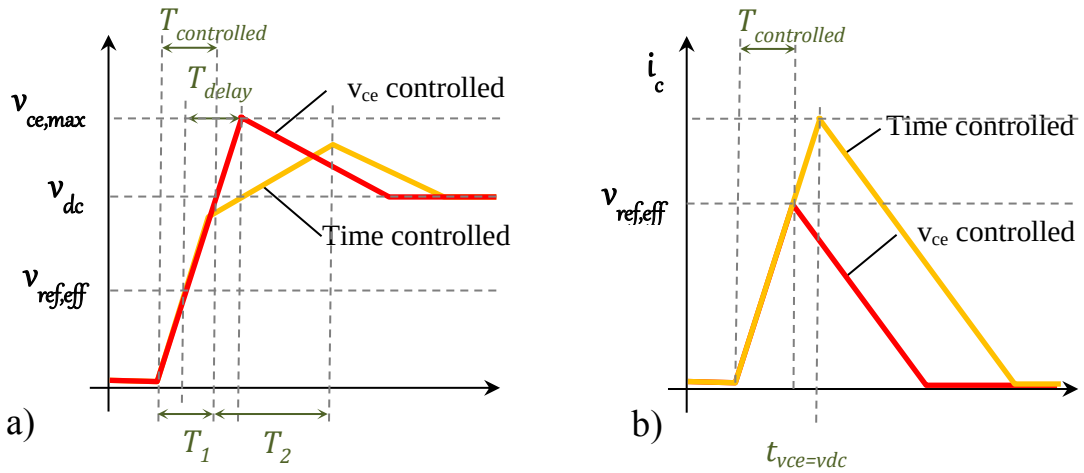


Fig. 41 *Voltage v_{CE} and i_c with v_{ce} controlled turn-off and time controlled turn off in the case of short-circuit event on the switching edge*

In the second mode, the switch S_4 is opened, from the instant when the short-circuit is detected, after a predetermined time interval T_1. Elapsed the time interval T_2 will open also the switch S_5 (cfg. *Fig. 41*).

The two methods exposed provide , circuit solutions that envolve different advantages and disadvantages. For this purpose, two different analysis will be conducted, divided by type of event, which are:

- short-circuit event on the switching edge,
- short-circuit event within the pulse.

Therefore, in the case of short circuit event on the switching edge it is apparent that, employing the v_{CE} controlled solution, at equal short-circuit current there is an increase of the overshoot voltage higher than 40% compared to that obtainable under normal operating conditions. This behavior is a direct consequence of an increase in the rise time of the IGBT gate voltage (in deep saturation mode). Vice versa, using the time-controlled solution there will have, a reduction in the overshoot voltage with an increase up to 10% of the collector peak current. This is a direct consequence of the feedback control, or depends on the minimum trip time (typically around 500ns).

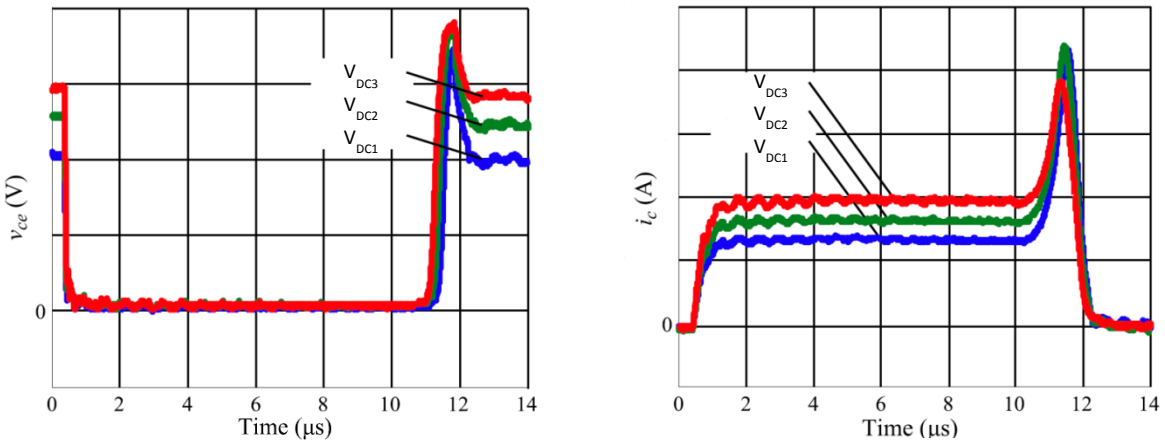


Fig. 42 *Voltage v_{CE} and i_c with v_{ce} controlled turn-off and time controlled turn off in the case of short-circuit event within the pulse, where there is $V_{DC3}>V_{DC2}>V_{DC1}$*

In the case of short circuit event within the pulse the overshoot voltage $\boldsymbol{v_{CE}}$ and the $\boldsymbol{i_c}$ collector peak current will grow together with the time interval after which the event occurs (cfg. *Fig. 42*).

7.2.4 Control Signal of the IGBT driver unit

The gate control unit provides two different status signals. The first signal shows the $\boldsymbol{v_{CE}}$ voltage edges that are provided by the state detection (cfg. *Fig. 33*). This signal is used to synchronize multiple switches connected in series. The second signal shows the $\boldsymbol{i_c}$ edges and is used to synchronize paralleled switches. These are obtained by an additional comparator connected to the integrator output.

1. *Current balancing in modulator with Multicore-transformer*

Due to tolerances in IGBT parameters, the geometry of the modulator and different propagation delays in driver circuits, a symmetric current balancing between the parallel connected IGBTs is not always guaranteed (cfg. *Fig. 43*). To ensure a safe operation the IGBTs have to be derated, which results in an oversized design. To achieve a better current balancing the manufacturer commonly preselects the IGBTs depending on the relevant parameters of the IGBT. But also after this costly classification the maximal power ratings of the IGBT must be reduced.

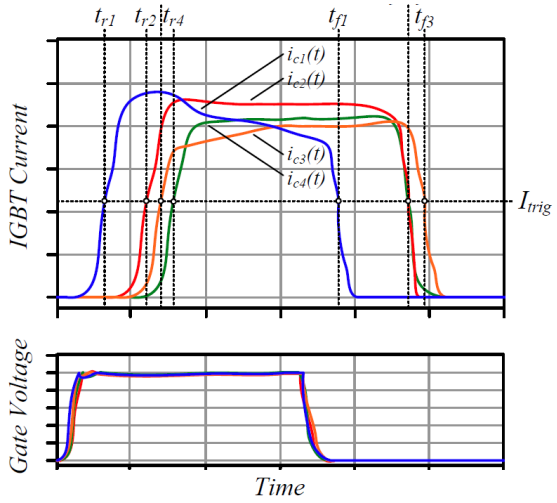


***Fig. 43** Example of IGBTs with unbalanced current waveform driven by equal gate voltage.*

Two different approaches can be used for achieving an equal current distribution and to avoid this derating. One possibility is to insert additional components, like series resistances or chokes, in the current path. The series resistances, however, result in additional losses and chokes slow down the rising and falling edges of the pulse.

Alternatively, the currents can be balanced with an active gate control. The only drawback of the active gate control is the need of a current measurement circuit for each IGBT, a more complex gate drive circuit and a parameter initialization before normal operation.

To balance the current among all IGBT modules, first the current is measured with a broad band current probe. Then, depending on the transient and static currents in each IGBT, the switching times and gate voltage of the individual IGBT are adjusted, which finally results in a balanced current distribution (cfg. *Fig. 44*).

In *Fig. 45* the schematic of a solid state modulator with several paralleled branches and the block diagram of the active gate control are shown. Each branch can be divided into a power and a control part. The power part consists of a storage capacitor $\boldsymbol{C_i}$, an IGBT module $\boldsymbol{S_i}$, a freewheeling diode $\boldsymbol{D_i}$ and a primary winding $\boldsymbol{P_i}$,

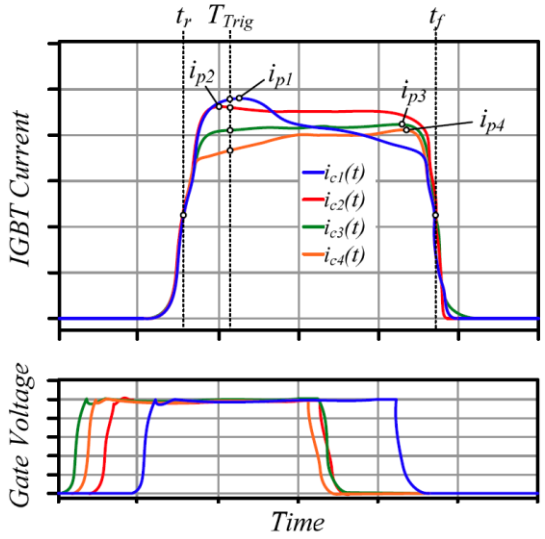


Fig. 44 *Examples for IGBT current pulses with synchronized rising and falling edges based on shifted gate signals.*

whereas the control loop embodies a gate drive circuit, a current probe and a measurement electronic for detecting the rise and fall times as well as the peak values of the current pulses. The control loop of each branch is closed with one control unit for all IGBT modules. Because, each IGBT, for a predefined trigger level $\boldsymbol{I_{trig}}$ of the collector current, is shown a different rising and falling time $t_{r1}\ldots t_{ri}$ / $t_{f1}\ldots t_{fi}$, before the next pulse is triggered the switching times and gate voltage of the individual IGBT are adjusted by the overall control system by translating it appropriately with respect to a master pulse.

The described impulsive currents balancing mechanism is intrinsically stable and is therefore able to guarantee, under operating conditions, compensation of the polarization currents drifts of IGBT with a positive temperature coefficient (e.g. Non-Punch-Through IGBTs).

Additionally, the absolute maximum values $\boldsymbol{i_{p1}}$ to $\boldsymbol{i_{pi}}$ of the IGBT current pulses are detected (cf. *Fig. 44*) and monitored, in order to guarantee balanced IGBT currents.

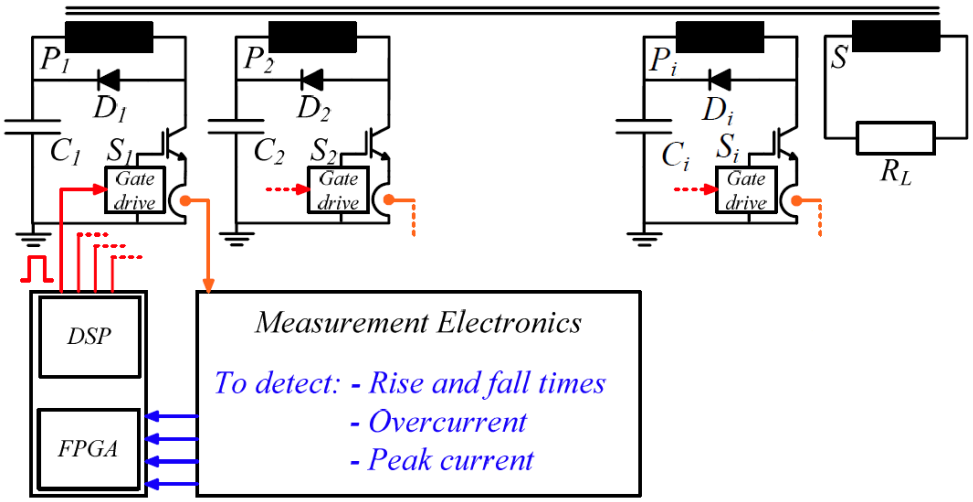


Fig. 45 *Block diagram of the modulator with active gate control.*

Before normal operation of the modulator the active gate control requires a few pulses at reduced output power, in order to determine the appropriate shift of gate signals and the amplitude of the gate signal, so that the currents are balanced.

The active gate control can be implemented on the DSP/FPGA board (cf. *Fig. 45*), which is also used for measuring the currents. This board performs the sampling of the signals coming from the measurement electronics in parallel. Due to the clock frequency of ADC (about thousand MHz) are possible the shifts of the gate voltage of a step about ten ns.

It is important to note that, in this type of control system, the propagation delay from the current probes to the DSP is not critical as long as the delays of all channels are the same, since a potential current unbalance is compensated just in the successive pulse.

The active gate control is initiated by the DSP, which triggers the gate drives at the beginning of the control sequence. Simultaneously, a counter is started on the FPGA. As soon as the rising and falling edges are detected, the FPGA stores the times of the corresponding event in the corresponding register (cf. *Fig. 46*).

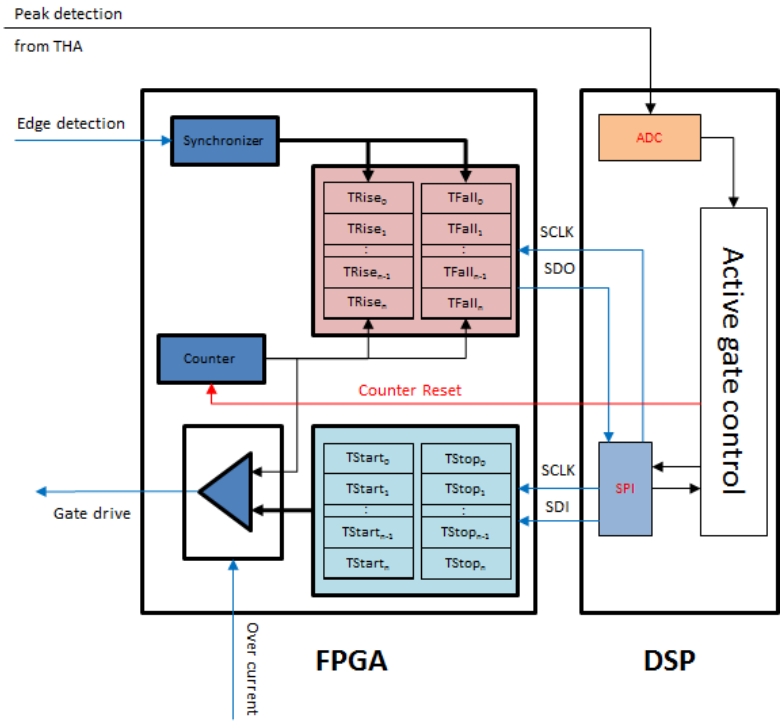


Fig. 46 *Block diagram of a possible active gate controller realized by FPGA/DPS architecture.*

Additionally, at the predefined time T_{Trig} the DSP samples the actual current values of each IGBT. Then, the DSP calculates the new turn on and off times, adjusts the gate voltage of each gate drive and is ready for the next pulse.

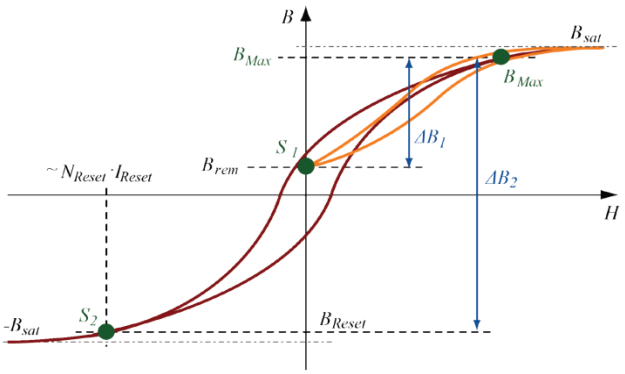


Fig. 47 *Example of unipolar flux swing (S_1 to B_{max})*

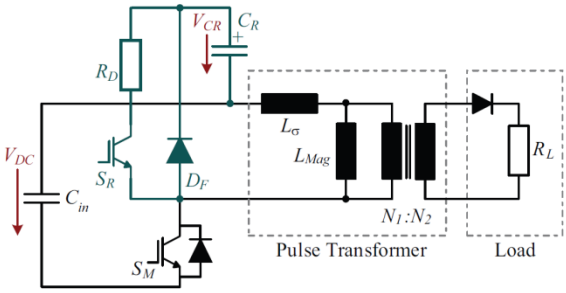


Fig. 48 *Schematic of the pulse modulator with the active reset circuit.*

7.3 Active premagnetization

In pulsed power systems utilizing pulse transformers for voltage conversion, the repetitive unipolar voltage pulses lead to a unipolar flux swing in the core material, as shown in *Fig. 47*. In this cases the core material of the pulse transformer is not optimally utilized and according to followed relations :

$$V_{DC} = N_1 \frac{d\Phi}{dt} = N_1 A_{Fe} \frac{dB}{dt}$$

$$A_{Fe} = \frac{V_{DC}}{N \frac{dB}{dt}}$$

The volume of the core will be about double that of a bipolar excitation for the same output pulse. A bipolar operation of the transformer could be achieved with a reset circuit - *dc reset* or *active premagnetization* - which premagnetizes the core to a negative flux density before the pulse is generated. The dc reset circuit leads to significant losses in the freewheeling. In order to reduce the losses and consequently the stress in the freewheeling diode path consists in recovering the energy stored in the magnetizing and leakage inductance of the transformer and reuse it in the next pulse. This leads to a significant reduction of the losses due to the premagnetization and an improved efficiency of the pulse modulator. It is important to note that active reset circuits can only be applied to power modulators operating on loads with a voltage-current characteristic such as that of a diode, because active magnetization requires that during the demagnetization phase the magnetic energy accumulated by the pulse transformer is not dissipated from the load but retrieved by a recovery capacitor.

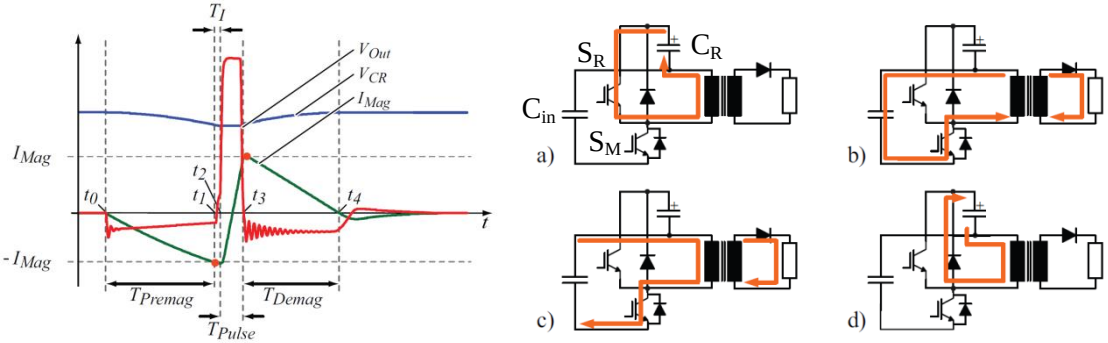


Fig. 49 *Current paths during a) the premagnetization time T_{Premag}, b) the interlocking delay T_I , c) the pulse duration T_{Pulse} and d) the demagnetization time T_{Demag}.*

During the premagnetization interval T_{Premag} the switch S_R is closed and the premagnetization current I_{mag} starts to flow in the primary winding of the transformer (cf. *Fig. 49*a). Current I_{mag} flowing in opposite direction as the load current generates a magnetic flux, which is in the opposite direction than the flux induced by the voltage pulse. Therefore, the energy stored in the capacitor C_R is transferred to the inductance L_{Mag} and if the capacitor is maintained at approximately constant voltage the corrispondent current I_{mag} will flow at a constant slope.

The S_R switch will be closed ($t = t_1$), as soon as the current in the transformer reaches its nominal value. However this will have to happen before that the switch S_M is in the on-state to prevent the capacitor of the pre-magnetizing circuit C_R is closed in short circuit with the capacitor of the pulse generator C_{in}. During the time interval T_1 in which both the two S_R, S_M switches are closed and the current will continue to circulate in the primary winding of the transformer through the freewheel diode of the S_M switch and the capacitor C_{in} (DC link). However, the magnetizing current due to the transformation ratio on the secondary will give rise to a very small current and an even smaller secondary voltage seen the dependency relationship (Child-Langmuir law) between voltage and current on the load.

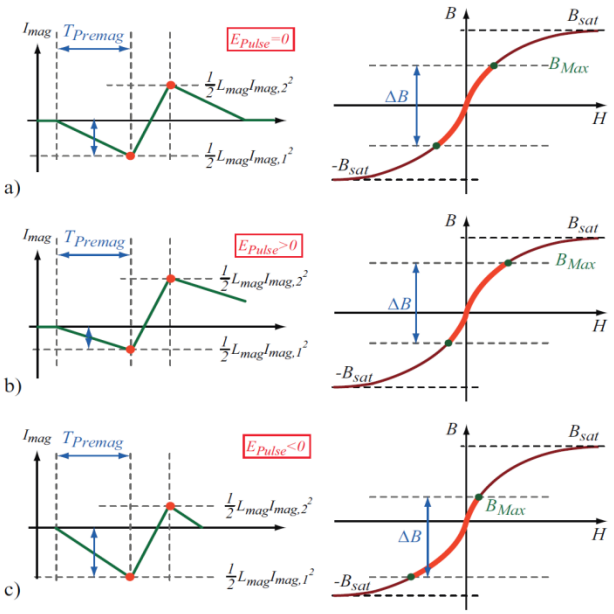


Fig. 50 *a) The energies after and before the pulse are the same, b) The energy after the pulse is the higher than the energy before the pulse and c) The energy after the pulse is the lower than the energy before the pulse .*

After the interlocking delay T_I at time instant t_2 the pulse is generate by turning on the main switch S_M. Then, the magnetizing current is linearly ramping up from $-I_{Mag}$ to I_{Mag} as shown in *Fig. 49* c) due to the constant pulse voltage V_{DC} . After the pulse, during T_{Demag} the energy stored in the magnetizing inductance L_{Mag} (and the part of the energy stored in L_σ, which is not dissipated in S_M while turning off) is fed back to the reset capacitor C_R via the freewheeling diode D_F *(cf.Fig. 49 d)*

In an ideal system without losses the energy recovered after the pulse will be the same as the energy, which was used to premagnetize the core. In this case the core is excited symmetrically from $-I_{Mag}$ to I_{Mag}.

Whatever the state of excitation of the core, in the absence of saturation of the magnetic flux density, the reset circuit is able to make the flux swing symmetrical.

In fact, for granted pre-magnetization time, results an asymmetric flux swing that leads an increase in the energy stored in the magnetizing inductance of the transformer ($E_{pulse}>0$). In the next cycle this energy will

be transferred into the reset capacitor increasing the voltage V_{CR} and then in turn by increasing the slope of the pre-magnetizing current so as to rebalance the asymetrical flux swing.

$$I_{Mag} = \frac{V_{CR} \cdot T_{Premag}}{L_{Mag}}$$

Conversely a decrease of energy accumulated in the inductance of magnetization ($E_{pulse}<0$) will be in the next cycle in a decrease of the voltage V_{CR} with consequent decrease in the slope of the pre-magnetizing current so as to rebalance the asymetrical flux swing.

In practice, however, due to losses in the diode D_F, in the switch S_R, in the bus bar, in the winding and in the core, not all of the pre-magnetizing energy is recovered, and therefore the voltage across C_R after each pulse not will reach the value that it had before the pulse. The voltage drop, caused by the system losses E_{Losses}, can be calculated by means of the difference of the stored energy in the capacitor C_R at t_2 and t_3 with the following relationship :

$$E_{Losses} = \frac{1}{2} C_R V_{CR,t2}^2 - \frac{1}{2} C_R V_{CR,t3}^2$$

which can be solved with $V_{CR,t3} = V_{CR,t2} - \Delta V_{CR}$

$$\Delta V_{CR} = V_{CR,t2} - \sqrt{V_{CR,t2}^2 - \frac{2E_{losses}}{C_R}}$$

Therefore in this case to ensure the balance of the flux swing is necessary that the following relation is satisfied:

$$\Delta E_{Pulse} = E_{losses}$$

where ΔE_{Pulse} is the variation of energy stored in the inductance L_{Mag} in turn equal to :

$$\begin{aligned} \Delta E_{Pulse} &= \frac{1}{2} L_{Mag} I_{Mag,2}^2 - \frac{1}{2} L_{Mag} I_{Mag,1}^2 \\ &= \frac{1}{2} L_{Mag} \left(\Delta I_{Mag}^2 - 2 \Delta I_{Mag} I_{Mag,1} \right) \end{aligned}$$

The above relationship means that the V_{CR} voltage across the reset capacitor result :

$$V_{CR,stable} = \frac{L_{mag}}{T_{Premag}} \cdot \left(\frac{\Delta I_{mag}}{2} - \frac{\Delta E_{Pulse}}{L_{mag} \Delta I_{mag}} \right)$$

which represents the voltage necessary to stabilize the system.

The latter relationship therefore highlights the fact that for low losses is possible to achieve the stabilization of the reset capacitor voltage by adjusting the pre-magnetising time or at most in the case of negligible losses by setting a pre-magnetizing interval and increasing the cross section of the magnetic core A_c. In the last case the pre-magnetizing interval must to unbalance slightly the flux swing so to accumulate more energy in the magnetizing inductance, and so to compensate the system losses ($\Delta E_{Pulse} = E_{losses}$).

In the case of pulse generator with large losses E_{losses} neither proposed solutions can be applied because a more asymmetric flux swing can lead to saturation of the transformer core or lead to an excessive increase in the size of the core.

The adoptable solution in this case constitutes a compensation of losses E_{losses} by resorting to a voltage regulation of the reset capacitor at a fixed value by the use of a DC/DC boost converter as shown in the circuit arrangement of *Fig. 51*. Also in this case acting on S_R and S_B switches will be possible not only to vary the pre-magnetizing interval but also the demagnetization interval.

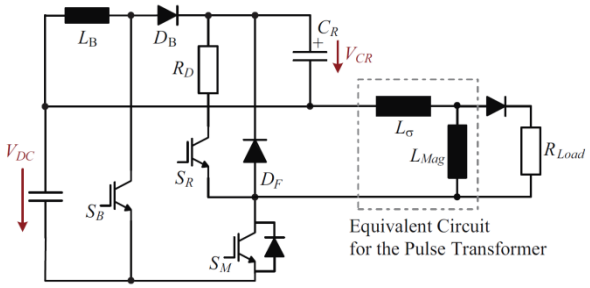


Fig. 51 *Schematic of the pulse modulator with the active reset circuit and DC/DC boost converter*

Therefore, by acting on the pre-magnetization time could be adjust the magnetizing current which obviously depends on the characteristics of the transformer and the applied load. Finally easily it shows that in the symmetrical excitation conditions, the two time intervals become equal in the hypothesis in which the forward voltage V_{DF} is neglected (cfc. *Fig. 50*).

$$T_{Premag} = \frac{L_{Mag} \cdot I_{Mag,1}}{V_{CR}}$$

$$T_{Demag} = \frac{L_{Mag} \cdot I_{Mag,2}}{V_{CR} + V_{DF}}$$

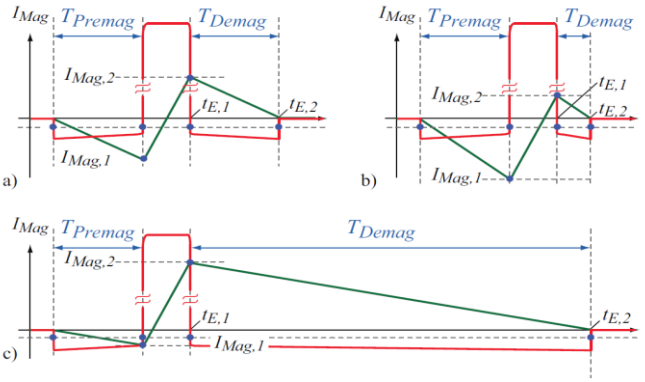


Fig. 52 *a) Symmetric flux swing, where $T_{Premag} = T_{Demag}$, b) and c) asymmetric flux swing, where is $T_{Premag} > T_{Demag}$ and $T_{Premag} < T_{Demag}$ respectively.*

In conclusion the active premagnetization circuit, since does not employ low-voltage auxiliary sources such as the passive premagnetization or the advanced premagnetization, will operate to the primary voltage of the pulse transformer to restore the energy lost in each cycle. Therefore, the DC/DC boost converter that will be used to restore the lost energy will employ swicth IGBT and not MOSFET at low voltage. This solution which at first sight could be more expensive in its construction leads to the following advantages:

- compact size of the premagnetizazion system, since it does not require the use of bulky choke induttance
- greater energy efficiency ($\eta \approx 98.9\%$),
- and simplest control law of the swicths.

7.4 Inductor Bouncer circuit

In the previous paragraphs, it has been repeatedly alluded to the difficulty of construction of HV modulator with small voltage drop on the output pulse. The main reason, as we shall see in detail in this section, due to the large electrostatic energy that is necessary to accumulate in the capacitor bank, and the requirements to these required in terms of parasitic characteristics.

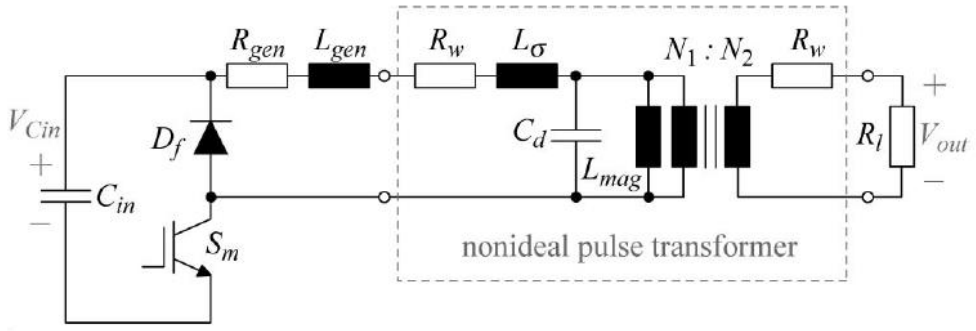


Fig. 53 *Simplified diagram of a pulse generator with its lumped parasites.*

In fact, the voltage droop is mainly defined by the input capacitance C_{in}, the pulse duration, and the output power. In some limit case, where the voltage droop Δ is limited to less than 0.1%, the stored energy E_{Cin} in the input capacitor C_{in} could be exceed the pulse energy E_p by more than 500 times in order to guarantee the specifications

$$\frac{E_{C_{in}}}{E_p} = \frac{\frac{1}{2}C_{in}V_{C_{in}}^2}{\frac{1}{2}C_{in}\left(V_{C_{in}}^2 - (1-\Delta)^2 V_{C_{in}}^2\right)} = \frac{1}{2\Delta + \Delta^2}$$

Therefore, on the one hand, the capacitor bank will get bulky and expensive, and on the other hand, a lot of energy is stored in the system, which could be a problem concerning safety aspects during a system fault.

One way to avoid the use of large storage capacitors to ensure low droop in the pulse is to employ appropriate compensation circuitry. In the long pulse modulators typically made in multistage configuration as Marx modulators the voltage droop can be corrected by switching appropriately stages of the modulator during the pulse flat top. In the short pulse modulators it is not possible to compensate the voltage droop employing additional switched-mode stages since the switching frequency request would imply a considerable increase of the losses. Furthermore it is unthinkable the use of RL networks that despite being easiest to realize they also would result a worsening of the overall performance of the modulator. A valid alternative to the above compensation circuitry is the use of an LC resonator in which the oscillation period is at least three orders of magnitude greater than the pulse duration. In this way the bouncer produces a pulse, that decreasing almost linearly is able to compensate the voltage droop (cfg. *Fig. 54*a). The way that in circuit allows to realize a resonant LC bouncer, through the use of standard semiconductor switches like the IGBT modules used in electric traction, is to use a Two-Winding Inductor Bouncer Circuit (cfg. *Fig. 54*b).

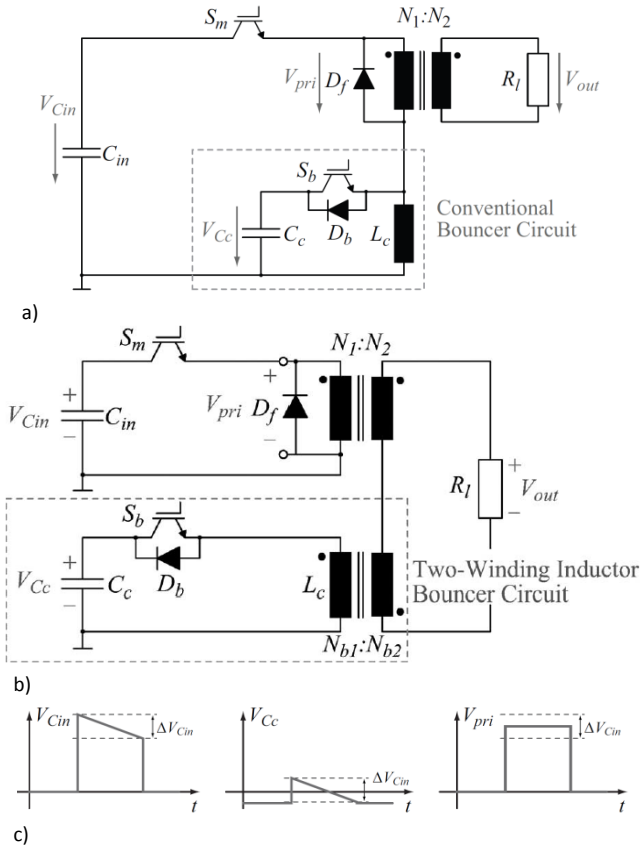


***Fig. 54** a) Conventional Bouncer circuit, b) Two-winding inductor bouncer circuit, c) Voltages $\mathbf{V_{Cin}}$ and $\mathbf{V_{Lc}}$ to achieve a constant output voltage $\mathbf{V_{out}}$.*

The resonant LC bouncer circuit, could be either placed on the primary side or on the secondary side of the pulse transformer. If the bouncer is placed on the primary side, the current through the switch of the bouncer must be higher than the current through the main switch during the pulse.

On the other hand, for a bouncer on the secondary side, the current through the bouncer switch is lower than for a bouncer on the primary side, but the switch voltage is much higher. In both cases, the design and the maximum voltage droop, that can be compensated, could be significantly limited by the semiconductors which are available.

To explain the operation of a bouncer circuit, the matrix transformer is first simplified to a transformer with one core and one primary/secondary winding. The resonant transition of the bouncer is split into three time intervals from T_1 to T_3 :

a) T_m: At the beginning of a pulse cycle, the two capacitors C_{in}' and C_c' are charged to $V_{C_{ino}}$, and $V_{C_{co}}$, and both switches are open. To initialize the pulse cycle, the bouncer switch S_b is closed, so that capacitor C_c' starts to discharge and the current i_{Lc}' in the bouncer inductor L_c' rises.

b) T_p: At the beginning of t_2, switch S_m is closed and the load current starts to flow. The load current has to flow through capacitor C_c' because the current in the bouncer inductance has to be continuous. The voltage across the bouncer capacitor still drops as long as the load current is smaller than the current through the bouncer inductance. Because the output pulse is centered around $\frac{T_B}{4}$, where T_B is the period of one resonant transition of the bouncer circuit, the voltage of the bouncer capacitor swings from a positive voltage to a negative voltage with applying the same peak value. Since, $v_{out}(t) = v'_{C_{in}}(t) + v'_{C_c}(t)$ the voltage across the load $v_{out}(t)$ is reduced by the bouncer at the beginning of the pulse and raised at the end of the pulse. This results in a more or less constant voltage across the load during the pulse.

c) T_d and T_r: At the beginning of t_3, the main switch S_m is opened, so that the bouncer is a pure parallel *LC* resonant circuit again. The bouncer capacitor voltage swings back to a voltage close to its initial voltage at the beginning of the pulse. At the end of T_r, the switch S_b is turned off to stop the oscillation at the zero crossing of the bouncer current.

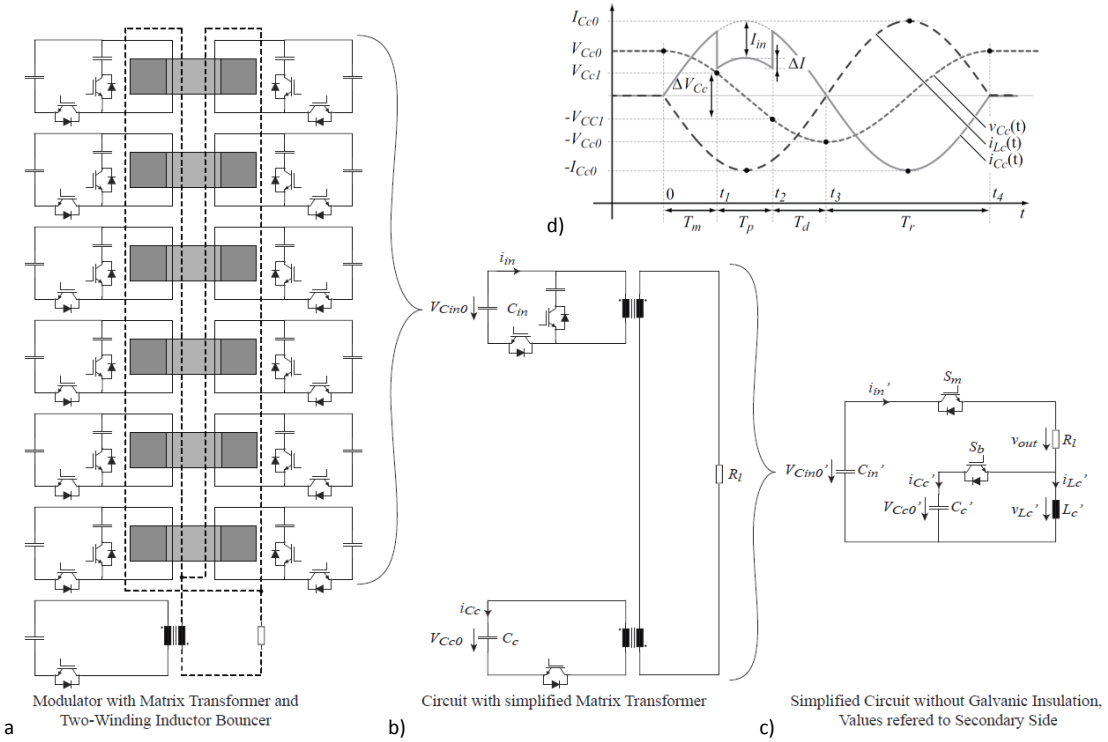


Fig. 55 *a)Modulator with Matrix Transformer and Two-Winding Inductor Bouncer, b) Circuit with simplified Matrix Transformer, c) Simplified circuit without galvanic insulation, d) Waveforms of the bouncer voltage* $\boldsymbol{V_{Cc}}$*, the capacitor current* $\boldsymbol{i_{Cc}}$ *and the inductor current* $\boldsymbol{i_{Lc}}$ *during one pulse period.*

The design of this subsystem requires the determination of simplified analytical reports in which will be neglected parasitic effects of the two-winding inductor. Therefore, it is assumed that, the insertion of the inductor, involves a transformation of the parameters of the circuit through the transformation ratio of N_{b1}:N_{b2}.

In order to achieve a constant output voltage $\boldsymbol{V_{out}}$, the drop voltage of the bouncer capacitor $\boldsymbol{V'_{Cc}}$ has to be equal to the input voltage droop $\boldsymbol{V'_{Cin}}$. In this case the output voltage is equal to the difference of the two initial voltages $\boldsymbol{V'_{Cin0}}$ and $\boldsymbol{V'_{Cc0}}$, which

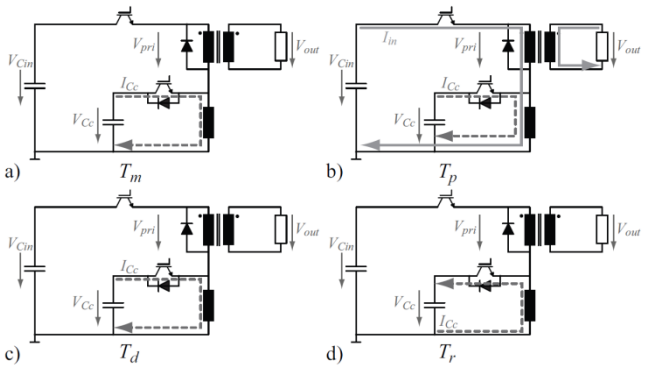


Fig. 56 *Voltages and current pathes during a) the magnetizing interval* T_m*, b) the pulse interval* T_p*, c) the demagnetizing interval* T_d *and d) the recovery interval* T_r *.*

results in a constant load current $\boldsymbol{I'_{in}}$.

$$I'_{in} = \frac{V'_{Cin0} - V'_{Cc0}}{R_l} = \text{constant}$$

Neglecting the parasitics, like magnetizing inductance or winding/interconnection resistances, the constant load current $\boldsymbol{I'_{in}}$ leads to a linear input voltage droop $\boldsymbol{V'_{Cin}}$.

$$\Delta V'_{Cin} = \frac{I'_{in} T_p}{C'_c}$$

However, since the bouncer basically is a resonant circuit, the current $\boldsymbol{i'_{Cc}(t)}$

$$i'_{Cc}(t) = I'_{Cc0} \cdot \sin(\omega t) - I'_{in}$$

with

$$\omega = \frac{1}{\sqrt{L'_c C'_c}}$$

in the bouncer capacitor $\boldsymbol{C'_c}$ has a sinusoidal run as shown in *Fig. 55d*. Additionally, the sine curve is shifted by the load current $\boldsymbol{I'_{in}}$ (cf. *Fig. 55*d and *Fig. 56*b) during the pulse. Assuming a relatively long period $T=2\pi/\omega=T_m+T_p+T_d+T_r$ of the resonance circuit compared to the pulse duration T_p, the current $\boldsymbol{i'_{Cc}(t)}$ in the interval $[T/4-T_p/2,T/4+T_p/2]$ can be assumed vary linearly, therefore, it can be written in the neighborhood of the peak current $\boldsymbol{I'_{Cc0}}$ at $t = T/4$

$$\Delta I'_{Cc} = i'_{Cc}(T/4) - i'_{Cc}(T/4 \pm T_p/2) = k_1 \cdot (I'_{Cc0} - I'_{in})$$

where k_1 is a proportionality factor between the current deviation $\Delta I'_{Cc}$ and the bouncer capacitor's peak current at $t = T/4$.

Thus, the needed resonance frequency:

$$\omega = \frac{2}{T_p} \arccos\left(\frac{i_{Cc}(T/4 \pm T_p/2)}{i_{Cc}(T/4)}\right) = \frac{2}{T_p} \arccos(1 - k_1)$$

of the bouncer circuit can directly be deduced based on the two current amplitudes at $T/4$ and at $T/4-T_p/2$ or based on k_1.

For a small deviation $\Delta I'_{Cc}$ this results in an almost linear voltage droop $\Delta V'_{Cc}$ during T_p, whereas the bouncer's capacitor voltage V'_{Cc} is symmetrically changing from V_{Cc1} to $-V_{Cc1}$ (cfg. *Fig. 55d*) or in other word :

$$2 \cdot \Delta V'_{Cc1} = \Delta V'_{Cin}$$

the bouncer's voltage droop of $2\Delta V'_{Cc1}$ during T_p can be expressed by the current $\boldsymbol{i'_{Cc}}$ (t), which is approximately $(I'_{Cc0} - I'_{in}) \cdot \sin(\omega t)$ during the pulse interval T_p , therefore

$$2 \cdot \Delta V'_{Cin} = \frac{1}{C'_c} \int_{T/4-T_p/2}^{T/4+T_p/2} i'_{Cc}(t)\,\mathrm{d}t = \frac{\bar{I}'_{Cc,Tp} \cdot T_p}{C'_c}$$

where $\bar{I}'_{Cc,Tp}$ is the average value of the current i'_{Cc}(t) during the pulse duration T_p, that can be written in linear approximation in this mode:

$$\bar{I}'_{Cc,Tp} = (I'_{Cc0} - I'_{in}) \frac{\sqrt{k_1(2-k_1)}}{\arccos(1-k_1)}$$

During T_m the stored energy in the inductor L'_c is completely delivered from C'_c , therefore, the required initial capacitor voltage V'_{Cc0} can be deduced from the energy balance:

$$\frac{1}{2} C'_c \left({V'_{c_{c0}}}^2 - {V'_{c_{c1}}}^2 \right) = \frac{1}{2} L'_c \left(I'_{c_{c0}} - \Delta I'_{c_c} \right)^2$$

The two-winding inductor bouncer has four degrees of freedom:

- Bouncer capacitance C'_c,
- bouncer inductance L'_c,
- initial bouncer voltage V'_{Cc0}
- and turns ratio of the two-winding inductor (bouncer transformer) N_{b1}:N_{b2}.

where the turns ratio is only used to adjust the current and voltage of the bouncer to values suitable for semiconductor switches at the end of the design process.

The bouncer circuit can be optimized for different quality criteria, as for example volume, losses, or the stored energy in the system.

However, the assumptions used, to extrapolate of the simplified project relationships, may give rise to circuit parameters that are hardly achievable or that are associated with parasitic effects no longer negligible. It is therefore essential to assess, for each circuit element obtained, the constructive tolerances that guarantee a droop voltage finish below the allowable.

This involves keep in mind that there are design constraints that must be respected and these are:

- the operational limits of the switch (maximum operating current and voltage)
- overall size of the inductors and capacitors (minimum oscillation frequency of the LC circuit),
- allowed droop voltage.

Therefore, it can be defined operationally on the plane L versus C a permitted region (Design Room) identified by four boundary curves (cfg. *Fig. 57*).

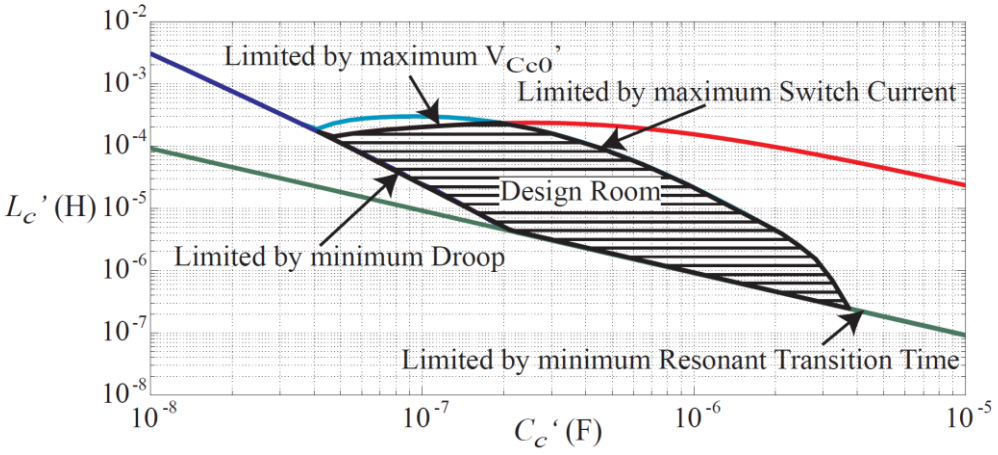


Fig. 57 *Design room for an assigned input capacitance C'$_{in}$*

Then, defined the design constraints and the optimization criteria, it is possible to obtain the values of the inductor and the capacitor by applying the following algorithms shown in *Fig. 58.*

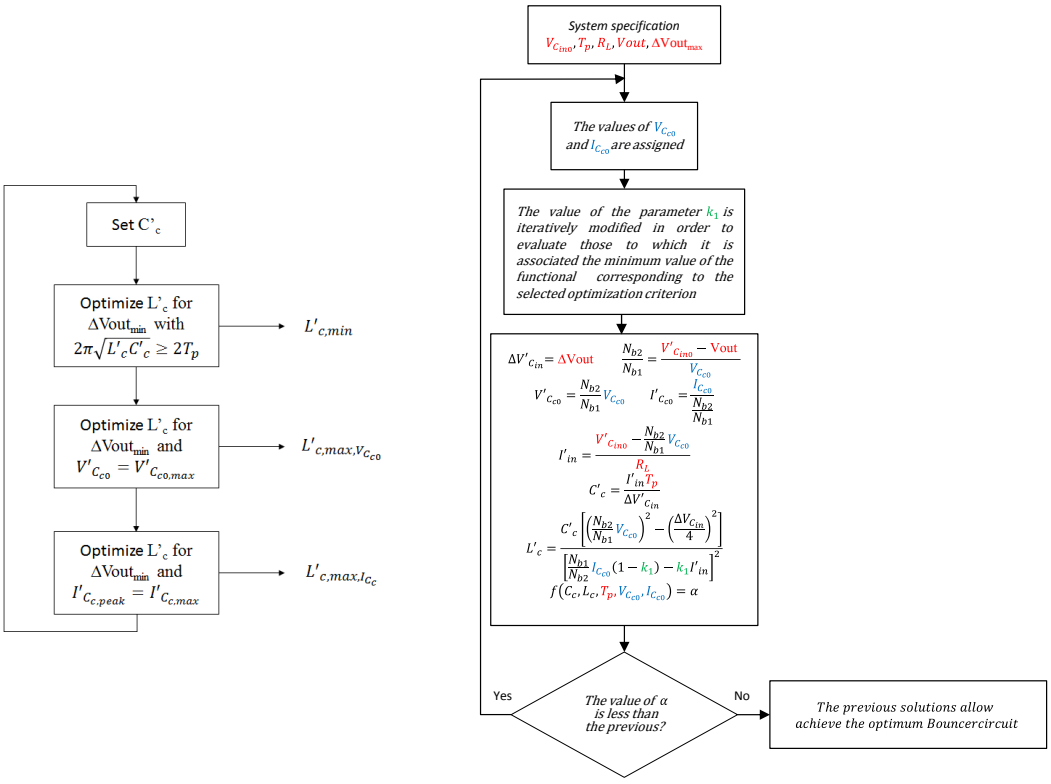


Fig. 58 *a) Algorithms used for calculation of circuit value limitations, b) Iterative workflow for optimizing the Bouncer circuit*

8 Pulse transformer

As already mentioned in an pulse modulator one of the most important and complex elements in its design is the pulse transformer.

In this section, we will begin to describe the main criteria that guide the designer in the sizing of a pulse transformer. The characteristic elements of a high voltage pulse transformer are:

- the output response to a pulse input,
- the capability to handle high voltages,
- the capability to handle electrodynamic and thermal loads corresponding to the nominal design power,
- the transformation efficiency.

The design criteria that we will be illustrating will aim to identify the parameters that need to manipulate in order to ensure conformity of the features of the transformer with the modulator design specifications.

8.1 Pulse shape design

To start, we will evaluate the criteria to be met to obtain an output pulse response, that matches the modulator specifications. Known, the equivalent lumped circuit of pulse transformer, it is possible to obtain an analytical model, which describes the corresponding output pulse response. In literature numerous electrical equivalent circuits considering LF and HF properties of pulse transformers have been proposed and IEEE standardized the equivalent circuit of pulse transformers [3] as shown in *Fig. 59* a). In order to simplify the analysis of the transient behavior for operation with rectangular pulse voltages, the standardized equivalent circuit can be reduced to the equivalent circuit *Fig. 59* b).

Therefore the first criteria has the objective to meet the specifications on the maximum overshoot and the maximum rise time.

According to the characteristic equations of the equivalent model shown in *Fig. 59* it is evident that in a first approximation ignoring

$$v_{out}(t) = \frac{V_g R_{load}}{R_g + R_{load}} \left[1 - e^{-at}\left(\frac{a}{k}\sinh(kt) + \cosh(kt)\right)\right]$$

with $k^2 = a^2 - b$ and

$$2a = \frac{R_g}{L_\sigma} + \frac{1}{C_d R_{load}}, \quad b = \frac{1}{L_\sigma C_d}\left(1 + \frac{R_g}{R_{load}}\right)$$

$$\sigma = \frac{a}{\sqrt{b}} \qquad T_r = 2\pi T_{10\%-90\%}\sqrt{L_\sigma C_d}$$

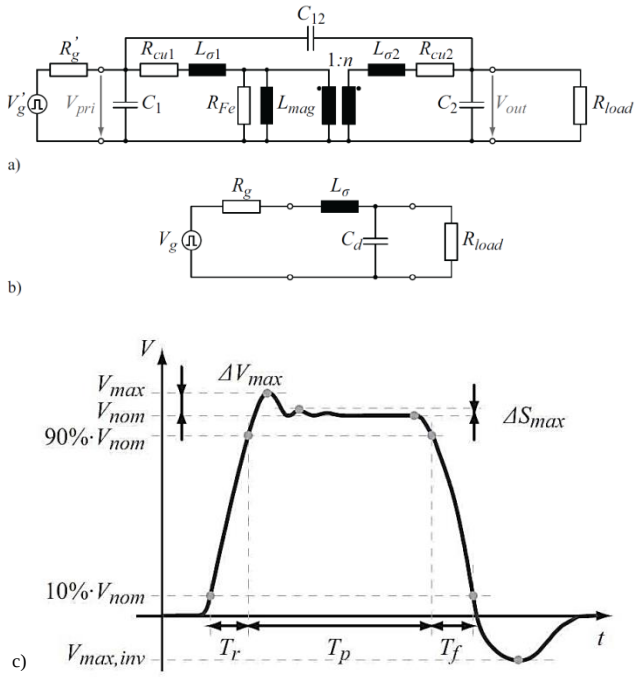


Fig. 59 *a) IEEE standardized equivalent circuit of a pulse transformer b) simplified equivalent circuit during the leading edge c) typical pulse waveform*

the effects of load and source, the maximum overshoot depends on the ratio between leakage inductance L_σ and the distributed capacitance of the transformer C_d, and the maximum rise time depends on the product between leakage inductance L_σ and the distributed capacitance of the transformer C_d.

In general, the pulse modulator connected to the transformer's primary, as well as, the load connected to the secondary winding, have respectively a certain inductance L_{gen} and capacitance C_{load}, which must to be considered. For the pulse generator a typical parasitic value of inductance of L_{gen} is content in a few hundred of micro Henry.

This means that the leakage inductance and the distributed capacitance of the transformer must be small to meet the pulse specifications.

In fact it results :

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma + L_{gen}}{C_d + C_{load}}}$$

$$T_r = 2\pi \cdot T_{10\%-90\%} \sqrt{(L_\sigma + L_{gen})(C_d + C_{load})}$$

where $T_{10\%-90\%}$ is a factor which depends on the damping coefficient σ *(cfc. Fig. 60)*.

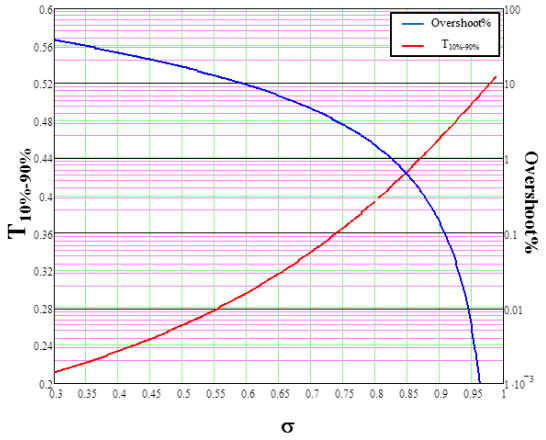


Fig. 60 *Overshoot and Normalized rise time vs the damping coefficient*

The ratio of L_σ and C_d, can be varied by the mechanical dimensions of the transformer, i.e. the distances, the heights and the lengths of the windings. The product of L_σ and C_d, however, is defined by the transformer topology and can be assumed to be approximately constant [4]. Therefore, the design criterion in this case is to choose the transformer topology which produces the smallest product $L_\sigma C_d$. Afterwards the designer will proceed to the mechanical design of the transformer, ensuring compliance with the other features, only at the end of the transformer sizing will be estimated the ratio L_σ / C_d.

In order to determine the topology of the transformer that gives rise to the smallest product $L_\sigma C_d$ is useful to analyze the *Tab. 4* where three different secondary winding topologies are examined (HV side winding).

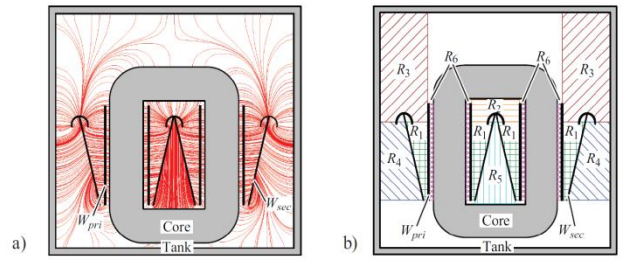
The values of L_σ and C_d, shown for each type of winding, are calculated respectively on the energy value of the electric field and the magnetic field stored between primary and secondary winding.

$$E_{mag} = \frac{1}{2}\mu \int_V \vec{H}^2 \, \mathrm{d}V \equiv \frac{1}{2} L_\sigma \cdot I_{pri}^2$$

$$E_{elec} = \frac{1}{2}\varepsilon \int_V \vec{E}^2 \, \mathrm{d}V \equiv \frac{1}{2} C_d \cdot V_{pri}^2$$

Limiting the calculation of the volume integral, only on the electric and magnetic fields into the gap between primary and secondary winding, can lead to an underestimate of the distributed capacitance and leakage inductance (underestimate overshoot).

In particular has been evaluated with different techniques (two-dimensional FEM simulation, mirror charges method), the difference of electrical energy stored by a transformer with a cone type secondary winding in the presence and absence of the tank. This analysis summarized in *Fig. 61* it showed an increase of electrical energy stored between the secondary winding and the tank (see region R_3 and R_4 in *Fig. 61*) at the expense of energy stored between the primary and secondary winding.



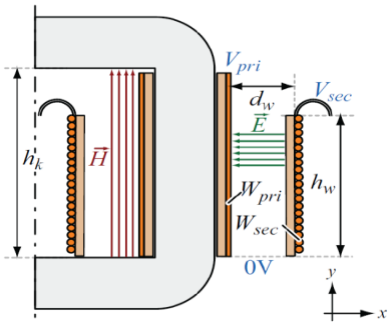
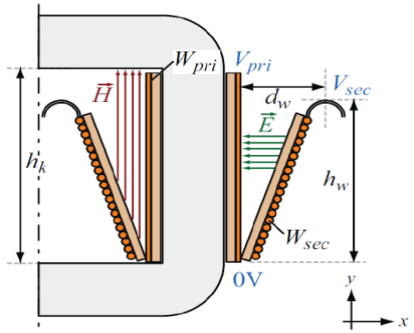
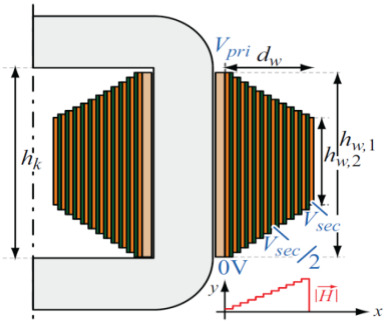
Region	R_1	R_2	R_3	R_4	R_5	R_6
With tank	22.6%	6.4%	44.4%	25.2%	0.6%	0.8%
Without tank	33.9%	9.6%	44.3%	10.1%	0.9%	1.2%

Fig. 61 *a) Electric field E of a transformer with cone winding in a tank. b) Six relevant regions for calculating capacitance C_d. In the table Relative stored electric energy of each region $R_1 \rightarrow R_6$ with and without tank.*

The equivalent electrical model of the transformer in this case is more complex because it manifests a capacitive effect between the secondary winding and tank no longer negligible. The same analysis was conducted for the estimation of the leakage inductances and the result of the comparison with a FEM simulation has given rise to a difference in the range between 10% and 20% if it is $d_w << h_w$ *(cfg. Tab. 4).*

These considerations therefore suggest to the designer that the use of simplified analytical reports of inductance and parasitic capacitance is not sufficient to validate the mechanical structure of the transformer, but they may be employed at a preliminary stage and then be validated using FEM methods.

In the HV pulse transformer a reduction of the $L_\sigma C_d$ product and the rise time T_r can be achieve with multiple cores transformer.

Parallel winding	Cone winding	Foil winding
		
		 $k = d_{cu}/d_{iso}$
$C_{d,parallel} = \frac{1}{3} \cdot \varepsilon \cdot \left(\frac{N_{sec}}{N_{pri}}\right)^2 \cdot \left(\frac{l_w \cdot h_w}{d_w}\right)$ $L_{\sigma,parallel} C_{d,parallel} = \frac{1}{3} \cdot \varepsilon\mu \frac{N_{sec}^2 \cdot l_w^2 \cdot h_w}{h_k}$	$C_{d,cone} = \frac{1}{2} \cdot \varepsilon \cdot \left(\frac{N_{sec}}{N_{pri}}\right)^2 \cdot \left(\frac{l_w \cdot h_w}{d_w}\right)$ $L_{\sigma,cone} C_{d,cone} = \frac{1}{4} \cdot \varepsilon\mu \frac{N_{sec}^2 \cdot l_w^2 \cdot h_w}{h_k}$	$C_{d,foil} = (k+1) \cdot \varepsilon \cdot \left(\frac{N_{sec}}{N_{pri}}\right)^2 \left(\frac{h_w \cdot l_w}{d_w}\right)$ $L_{\sigma,foil} C_{d,foil} = \frac{k+1}{2} \cdot \varepsilon\mu \frac{N_{sec}^2 \cdot l_w^2 \cdot h_w}{h_k}$
	Smallest $T_r = 2\pi T_{10\%-90\%} \sqrt{L_\sigma C_d}$	

Tab. 4 *Different type of secondary winding and the main relationship of the corresponding leakage inductance and distributed capacitance.*

8.2 Electro-mechanical design

The mechanical design of a matrix transformer is an iterative process that starts with the following specifications:

- Input voltage and current
- Output voltage and current/power
- Frequency of operation
- Maximum core temperature or temperature rise
- Environment temperature
- Pulse length

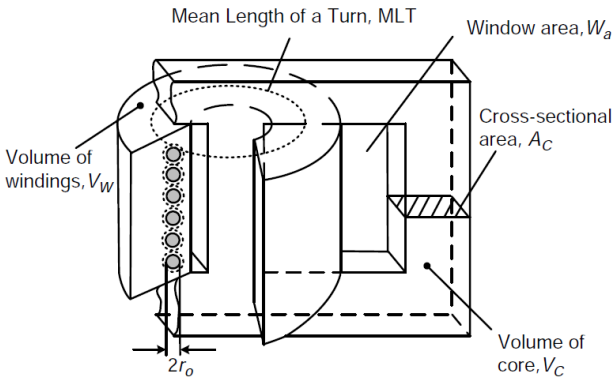


Fig. 62 *Typical layout of a transformer*

that allow to select most suitable magnetic material to its realization. This last will characterized by appropriate constitutive parameters provided by the manufacturer (B_{sat}, K_c, ρ_c, α, β) that will allow to calculate the maximum magnetic flux B_o, the physical dimensions of the transformer (W_a , A_c , MLT), the number of primary and secondary winding turns, the corresponding current density J_o of windings and therefore the physical dimensions of the conductors of the windings.

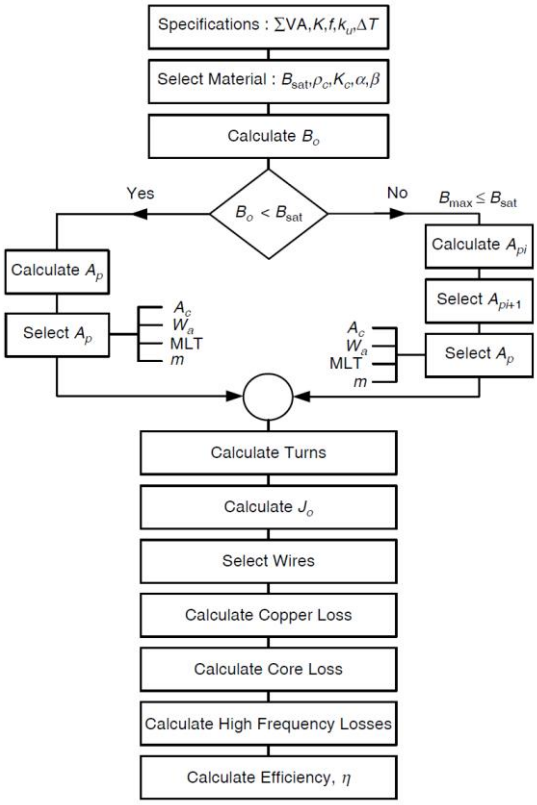


Fig. 63 *Flow chart of design process.*

Obviously the physical size of a HV pulse transformer must also respect insulation specifications which depend on the application of the relevant safety standards. The widely used standards that are relevant to the insulation requirements in power supplies and its transformers for office and household applications are IEC60950 and IEC60335.

At the end of this iterative process will be determined the Copper loss, the Core loss, the high frequency loss and the equivalent lumped parameters of the corresponding transformer. The design therefore consist into operate iteratively following the steps indicated in the flowchart shown in *Fig. 63* and based on the results obtained at the end of each cycle make the corrections that involve compliance with the design specifications on the impulse response of the transformer (time rise, overshoot voltage, droop voltage).

As shown in the flowchart the first step is to identify the core material, in fact non-ideal properties of the magnetic material ($\mu \neq \infty$) directly influence the performance of the pulse transformer in terms of maximum power transferred to the load ***ΣVA*** and transient response.

For example with a higher B_{max}, the core cross section can be reduce, which results in smaller parasitic effects and therefore in faster rise times.

About that in the *Tab. 5* is shown the maximum flux density B_{max} according to the concentration of certain constituent elements of the iron alloy.

Despite the existence of ferromagnetic materials that show the highest flux densities such as cobalt-iron alloys is necessary to select materials with low core losses. Therefore, the ferromagnetic alloys most commonly used in the realization of pulse transformers are those with amorphous material and nanocrystalline structures such as silicon-iron alloys which besides showing low core losses are also less expensive.

Core materials and maximum flux density B_{max}

CoFe (35%-65%)	2.43T
Fe	2.16T
SiFe (3%)	2T
Ni (75%)	0.6T
NiFe (50%-50%)	1.6T

Tab. 5 *Core materials and maximum flux density*

However, the core losses are not only defined by the selected material. The thickness of the metal tape used in tape wound cores or the pulse duration, as shown in *Fig. 64*, can strongly influence the core losses.

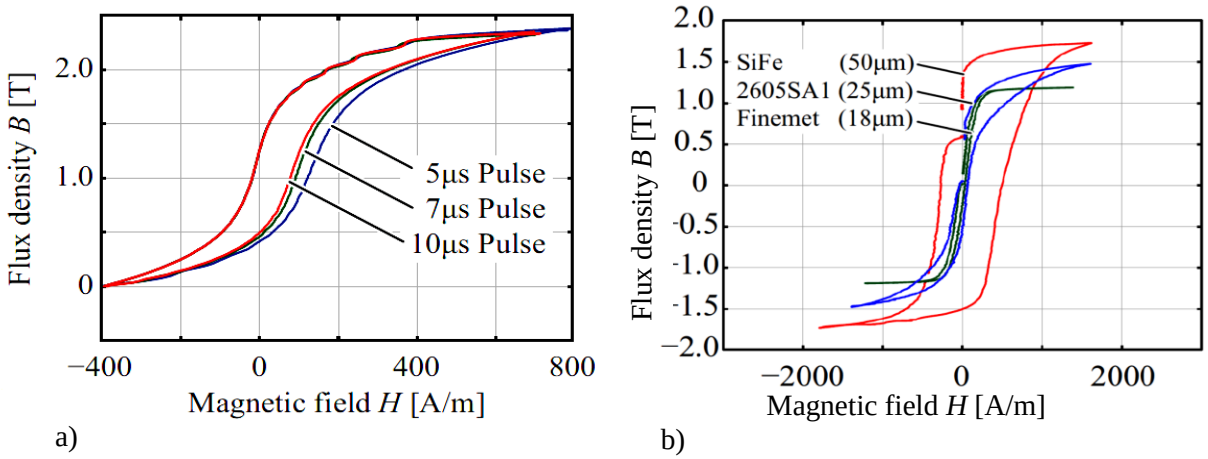


Fig. 64 *Measured hysteresis curve of a) of 2605SA1 for different pulse durations of 5 µs, 7 µs and 10 µs and b) SiFe alloy with tape thicknesses of 50 µm, 2605SA1 alloy with tape thicknesses of 25 µm, Finemet alloy with tape thicknesses of 18 µm.*

As shown in flowchart the first step to be performed, after the choice of the ferromagnetic material of the core, is the calculation of the optimum value of the magnetic flux density. The optimum flux density is a function of the total losses (see *Fig. 65*) therefore can be envisaged the following two possible cases:

- the optimum flux density is not limited by the saturation flux density,
- the optimum flux density is limited by the saturation flux density.

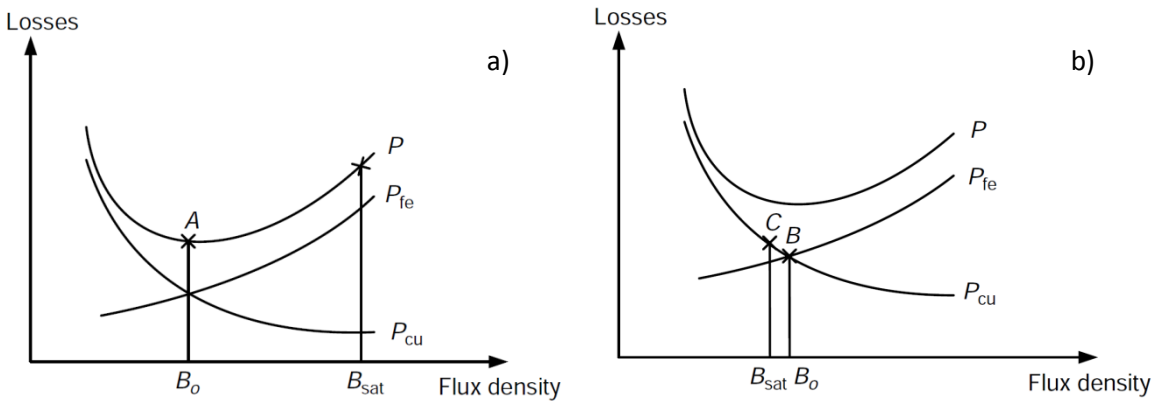


Fig. 65 *a)Winding, core and total losses unlimited by saturation*
b) Winding, core and total losses limited by saturation

In the case where the optimum flux density is not limited by B_{sat}, (cfg. *Fig. 65*b) it is possible to make some simplifying assumptions, which allow to evaluate a dimensional parameter which depends on the apparent power required by the load and depends on the constituent parameters of the magnetic material employed. This parameter is obtained by the product of the *core cross-sectional area* A_c and the *window winding area* W_a. It is an indication of the core size, and is designated *window-cross-section product* A_p.

The initial value of A_p is given by following equation :

$$A_p = \left[\frac{\sqrt{2}\sum \mathrm{VA}}{K_v f B_o k_f K_t \sqrt{k_u \Delta T}}\right]^{8/7} \qquad \text{[A7]}$$

where the K_t is the *waveform factor* that for a typical shape of a pulse value :

$$K_V = \frac{RMS}{ARV} = \frac{1}{2}\sqrt{\frac{D}{\frac{tr}{\tau}\left(D-\frac{tr}{\tau}\right)}}.$$

For simplicity of analysis we will assume hereinafter that the optimal flux density is not limited by saturation (cfg. *Fig. 65*a). In this circumstance the optimum flux density is obtained in correspondence to the value for which the total loss is twice the copper loss (at point *A* in *Fig. 65*a, the core loss is equal to copper loss). Remembering that at fixed frequency the total loss is to be:

$$P_{\mathrm{cu}} + P_{\mathrm{fe}} = \frac{\beta+2}{\beta} P_{\mathrm{cu}}$$

and will have :

$$\beta = 2$$

Moreover since it results:

$$P_{\mathrm{cu}} = \rho_w V_w k_u J_o^2$$

ρ_w electrical resistivity of the conductor

k_u window utilization factor[A8]

[A7] The optimum design criterion using the equations for copper loss P_{cu}, core loss P_{fe} and thermal heat transfer.

[A8] The *window utilization factor* k_u in the case of HF pulse transformers take into account the *skin effect* in conductors and the occurrence of the *proximity effect* between conductors. In fact in both cases there is an increase of the

V_w volume of the windings

then using the thermal equation:

$$P_{\text{cu}} + P_{\text{fe}} = \frac{\beta + 2}{\beta}\left[\rho_w V_w k_u J_o^2\right] = h_c A_t \Delta T$$

h_c the coefficient of heat transfer
A_t convective surface area

It is possible extracting the current density:

$$J_o = \sqrt{\frac{\beta}{\beta + 2}\frac{h_c A_t \Delta T}{\rho_w V_w k_u}}$$

Employing the dimensional analysis equations for A_t *(convective surface area)*, V_c *(volume of the core)* and V_w *(volume of the windings)* :

$$V_w = k_w A_p^{\frac{3}{4}}$$

$$V_c = k_c A_p^{\frac{3}{4}}$$

$$A_t = k_a A_p^{\frac{1}{2}} \quad \text{[A9]}$$

and taking $\beta = 2$ gives an expression for the current density in terms of the temperature rise in the windings and the core-window winding area product:

$$J_o = K_t \sqrt{\frac{\Delta T}{2k_u}}\frac{1}{\sqrt[8]{A_p}}$$

where K_t is defined as :

$$K_t = \sqrt{\frac{h_c k_a}{\rho_w k_w}}.$$

Therefore the optimum value of the flux density will be:

$$B_o = \frac{[h_c k_a \Delta T]^{\frac{2}{3}}}{2^{\frac{2}{3}}[\rho_w k_w k_u]^{\frac{1}{12}}[k_c K_c f^{\alpha}]^{\frac{7}{12}}}\left[\frac{K_w f k_f k_u}{\Sigma \text{VA}}\right]^{\frac{1}{6}} \quad \text{[A10]}$$

---

winding resistance that results from a reduction in the effective area of conduction. Therefore, this factor is the ratio of the total conduction area W_c for all conductors in all windings to the total window winding area W_a of the core:

$$k_u = \frac{\sum_{i=1}^{n} N_i A_{wi}}{W_a}$$

where A_{wi} is the conducting area of the wire in winding i. Typically this expression giving k_u=0.4.

[A9] Note that the volume of the winding (fully wound $k_u = 1$) is given by

$$V_w = MLT(\text{Mean Length of a Turn}) \times W_a,$$

and the volume of the core is $V_c = l_c \times A_c$ where l_c is the length of the magnetic core.

[A10] In the case of laminated and tape-wound cores, the effective cross-sectional area of the core is less than the physical area, Ac, due to interlamination space and insulation. For this purpose is defined a *stacking factor* k_f by the following relationship:

$$A_m = k_f A_c$$

A typical value of this factor is : $k_f = 0.95$

The optimum flux density (RMS value) may be found from the specifications of the application and the material constants. Once we know the optimum flux density it is possible to obtain the *core-winding window product area* A_p.

In the case where it is required to comply with more stringent constraints on the peak output voltage and the rise time of the pulse response, the method described, has little applicability since, has as its sole objective to obtain the best electrical efficiency at thermodynamic equilibrium conditions.

The design method that will be described and applied in the next chapter will instead ensure compliance with the latest constraints and this will help:

- minimize the maximum electrostatic energy stored in the transformer by reducing as much as possible the dimension
- minimize the magnetic energy, by reducing as much the number of primary and secondary coils as possible and using a multi-core magnetic configuration.

In this circumstance, to optimize the sizing of the transformer, is necessary to apply a new criteria that will be described briefly here in anticipation of a forthcoming publication in the specialized magazine. The above criterion provides a semi-analytical estimate total electrostatic energy accumulated by the transformer and an iterative procedure in the determination of certain salient parameters (number of primary turns and a free geometrical parameter).

The design equations which allow to define the cross-section of the ferromagnetic core are derived directly from the following law of Faraday Neumann Lenz :

$$v_p(t) = N_p \frac{dB}{dt} A_c$$

In fact, for assigned:

- peak voltage on the primary windings $V_{p_{peak}}$ (imposed by design choices on the semiconductor devices used to realize the pulse generator),
- pulse duration τ ,
- maximum magnetic flux density B_{max}

it will be:

$$N_p \cdot A_c = \frac{V_{p_{peak}}}{2 \cdot B_{max}} \tau$$

from which the product turns per cross-sectional area of the magnetic core will remain bonded.

In order to decouple the latter, is necessary to identify the other geometric parameters that remain bound to the maximum voltage and the maximum desirable parasitic capacitance on the secondary winding. The main geometrical parameters which are bound to the secondary winding voltage are:

- the minimum distance between the secondary winding and the primary winding $d_{w,min} + d_{wb}$,
- the minimum distance between the secondary winding and the walls of the oil tank $d_{w,min}$,
- the minimum distance between coils of the secondary winding d_{sts}.

The first step of the project criterion, as anticipated, is to reduce the maximum electrostatic energy that can be accumulated by the transformer or to find geometric configurations that limit high-electric areas and consequently reduce the overall size of the transformer.

For that purpose, the conductor of the secondary coil with the higher voltage potential is usually realized by a guard ring with a radius R_r, this operation reduce the distance between the secondary winding and the tank walls or the primary winding.

In fact, this solution compared to that of two parallel planes electrodes involves the following differences:

- high surface electric fields on the higher electric potential surfaces,
- less electrostatic energy stored and consequently lower parasitic capacitances

obviously this latter statement is true as long as the radius of the conductor R_r gives rise to an electric field greater than that produced by two parallel faces.

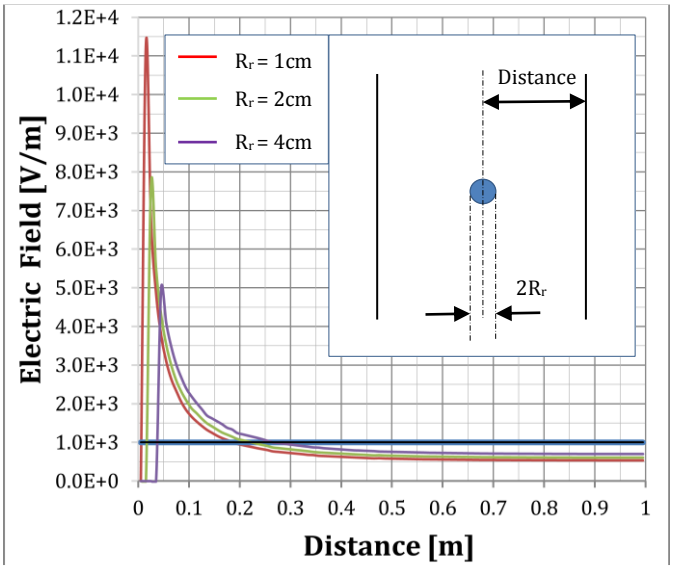


Fig. 66 *Radial electric field produced by a guard ring vs. the diameter 2**R**r and the position **Distance** (**$V_{guard} = 1kV$**)*

In *Fig. 66* as examples it has been reported the trend of the electric field for different diameters $2R_r$ of the cylindrical conductor , while in *Fig. 67* is shown the trend of the linear density of electrostatic energy for different diameter of the cylindrical conductor but to assigned potential difference and distance of the electrodes. From this last graph, it is possible to observe that, for given distance between the electrodes and the electrical potential difference, exists a diameter $2R_r$ of the cylindrical conductor in correspondence to which the electrostatic energy stored is equal to the configuration with planar electrodes.

In addition, in correspondence to the above diameter, the maximum electric field at the surface will be equal to that of a configuration with planar electrodes but with a consequent lower electric field distribution and lower total electrostatic energy.

Therefore, on the basis of these observations, it is possible to construct a family of curves that, for granted maximum electric field and the potential difference between the electrodes, allows to calculate the diameter $2R_r$ and the minimum safety distance $d_{w,min}$.

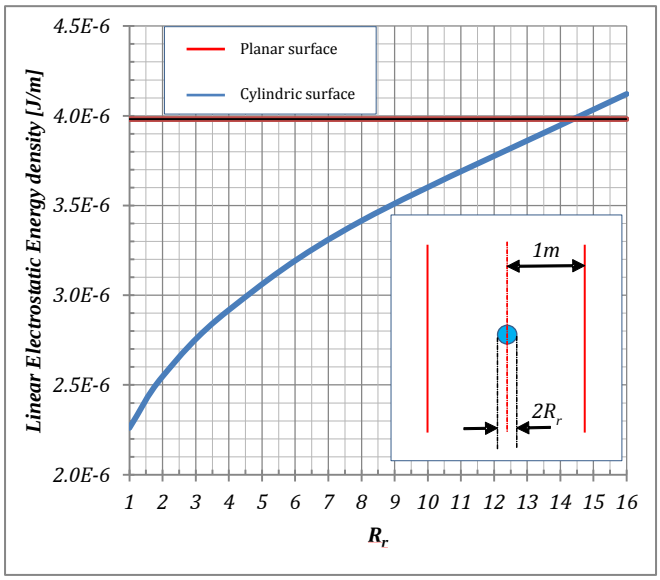


Fig. 67 *Linear electrostatic energy density vs the diameter* $2\boldsymbol{R_r}$ *of the guard ring (Distance=1m,* $\boldsymbol{V_{guard} = 1kV}$*)*

In *Fig. 68* are shown diagrams that allow to evaluate the minimum safety distance $d_{w,min}$ between the guard ring and the walls of the oil tank while in *Fig. 69* are shown diagrams that allow to evaluate the safety distance between adjacent turn coils of the secondary winding $d_{sts,min}$. The analytic relationships that must be considered to construct the design charts shown in *Fig. 68* and in *Fig. 69* are:

$$E(R_r) = \frac{V_s}{R_r} \frac{1}{ln\left(\frac{d_{w,min}}{R_r}\right)}$$

$$E_{av} = \left(\frac{V_s - V_p}{d_{w,min} - R_r}\right)$$

where is assumed that the radial electrical field $E(R_r)$ and average electrical field E_{av} of an equivalent pair of planar electrodes are equal to 16kV/mm, which it is the tolerable value of the maximum electrical field in oil for medium length pulses (50μs).

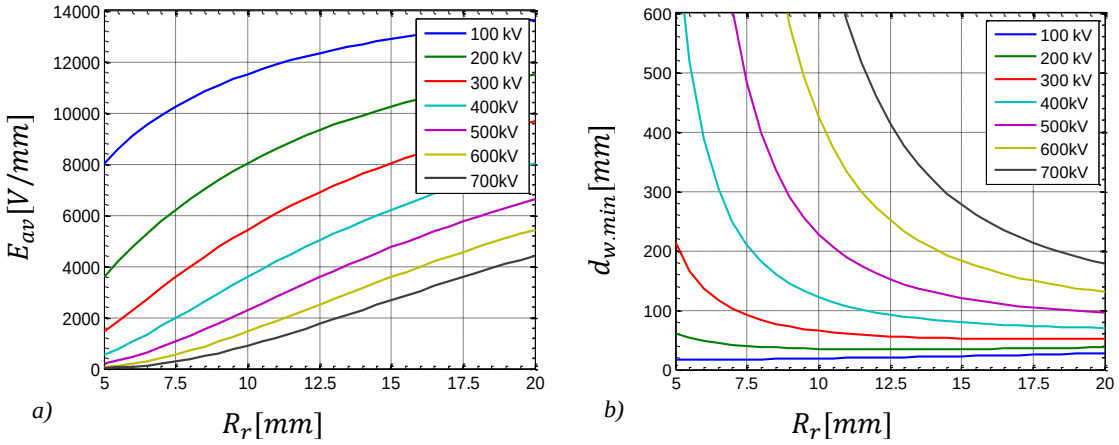


Fig. 68 *a) Minimum average electric field* $\boldsymbol{E_{av}}$ *corresponding to the minimum safety distance* $\boldsymbol{d_{w,min}}$ *as a function of* $\boldsymbol{R_r}$ *size and the maximum secondary voltage* $\boldsymbol{V_s}$ *; b) minimum safety distance* $\boldsymbol{d_{w,min}}$ *from the guard ring of the magnetic core as a function of* $\boldsymbol{R_r}$ *size and the maximum secondary voltage* $\boldsymbol{V_s}$*.*

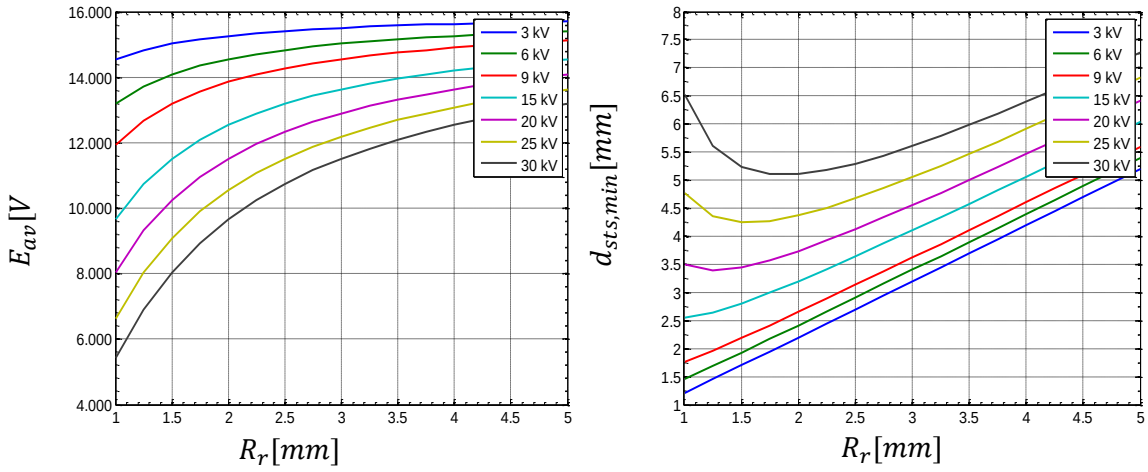


Fig. 69 *a) Minimum average electric field* $\boldsymbol{E_{av}}$ *corresponding to the minimum safety distance* $\boldsymbol{d_{w,min}}$ *as a function of* $\boldsymbol{R_r}$ *size and the maximum secondary voltage* $\boldsymbol{V_s}$ *; b) minimum safety distance* $\boldsymbol{d_{w,min}}$ *from the guard ring of the magnetic core as a function of* $\boldsymbol{R_r}$ *size and the maximum secondary voltage* $\boldsymbol{V_s}$.

Therefore, the electromechanical design of a HV pulse transformer, once selected the ferromagnetic material that ensures the highest possible magnetic flux density, continues with the estimation of the following geometrical parameters:

- $d_{w,min}$,
- R_r,
- $d_{sts,min}$

on the basis of the dielectric strength of insulation oil and of the maximum voltage on the secondary winding.

The estimate of $d_{w,min}$ allows to fix the distance between the secondary winding and the tank walls and consequently the distance between the primary winding and the secondary winding ($d_{w,min} + d_{wb}$).

At this point it is possible to start the iterative process of the project, which presupposes at each cycle the choice of the number of turns of the primary windings N_p and consequently of the secondary windings N_2 , in fact is :

$$N_2 = N_p \cdot n_{Turn} \qquad n_{Turn} = \frac{V_2}{V_1}\frac{1}{n_{core}}$$

where n_{core} is the magnetic core number of the matrix transformer.

Chosen the number of primary turns will be possible to calculate the *cross section area* A_c of each magnetic core.

$$A_c = \frac{V_{p_{peak}}}{2 \cdot N_p \cdot B_{max}}\tau$$

Another hypothesis we will make to simplify the iterative process is to assume that the primary winding consists of a single layer, so it will be easier to estimate the size of the *window windings area* W_a.

In fact, according to the geometry parameters shown in *Fig. 70* will have:

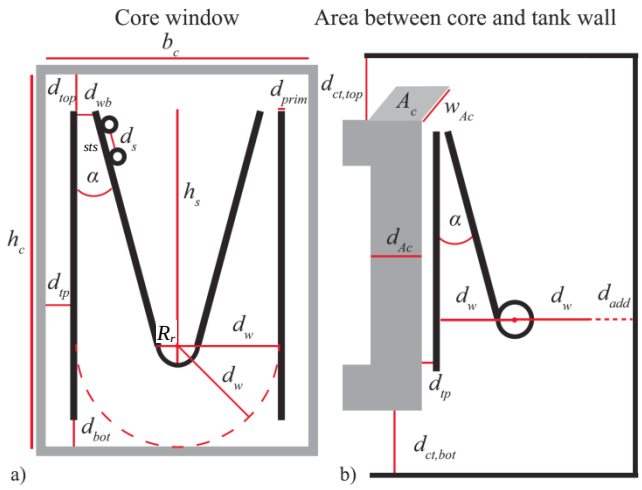


Fig. 70 Geometric setup of the transformer.
(a) Geometric variables in the core window.
(b) Geometric variables between core and tank wall.

$$d_{top} = d_{tp} + R_{Fillet}$$

$$h_s = \frac{d_w}{tan(\alpha)}$$

$$b_c = 2 \cdot \left(R_r + d_w + d_{wb} + d_{prim}\right) + 3 \cdot d_{tp}$$

$$h_c = \frac{3}{2} d_w + h_s + d_{top}$$

$$W_a = b_c \cdot h_c$$

The estimate of the *window windings area* W_a allows together with the *cross section area* A_c to define the dimensional parameter *core-winding window product area* A_p thanks to which is also possible to evaluate the *optimal current density* J_o in thermodynamic equilibrium state.

The relations to be used to evaluate A_p and J_o are the following:

$$A_p = A_c \cdot W_a$$

$$J_o = K_t \sqrt{\frac{\Delta T}{2k_u} \frac{1}{\sqrt[8]{A_p}}}$$

where K_t is defined as :

$$K_t = \sqrt{\frac{h_c k_a}{\rho_w k_w}}.$$

and where the relationship of the *optimal current density* is evaluated in thermodynamic equilibrium condition between the thermal energy produced in the magnetic core and in the windings and the heat transferred mainly by convection to the coolant fluid.

The estimate of the *optimal current density* J_o will allow to evaluate the consistency of dimensional choice of the primary winding d_{prim} and the secondary winding conductor r_{ws}.

Once the geometry parameters of the transformer are defined, it will be possible to calculate the equivalent circuit parameters (L_σ , C_d) and accordingly evaluate the most appropriate action to take to obtain the desired impulse response.

In fact, the rise time and the overshoot (pulse requirements) depend on the total inductance and capacitance therefore the geometrical parameters of the pulse transformer (b_c,h_s,h_c,d_{Ac},α) will be optimized in order to obtain the threshold values indicated in the previous paragraph. In *Fig.71* is shown the iterative process that is applied, in the design of a pulse transformer, to obtain the optimal pulse shape.

The total capacity shown by the transformer to the pulse generator also depends on the capacitance of the load C_L applied to the secondary of the transformer (e.g., the capacity of the tube device and/or a capacitive

voltage divider), in fact the contribution of the parasitic capacitor results at the primary winding $n_{core} \cdot n_{Turn}{}^2 \cdot (C_L + C_d)$.

Vice versa, the total inductance depends on the equivalent leakage inductance L_σ and the pulse generator inductance.

The space between the primary winding and the secondary winding, affect in the same way the average turn length of the winding and then L_σ and C_d. Therefore, the rise time that depends on the turn length can be reduced chosen a square-shaped turn of the winding.

The regions outside the area between the primary winding and the secondary winding also contribute significantly to C_d but not to L_σ. In the case of grounded windings connected to the ground, total capacity could be reduced by decreasing the total volume of the tank, always observing the safety distances due to the peak voltage of the secondary winding. The optimization of tank dimension however required a 3D-FEM simulation.

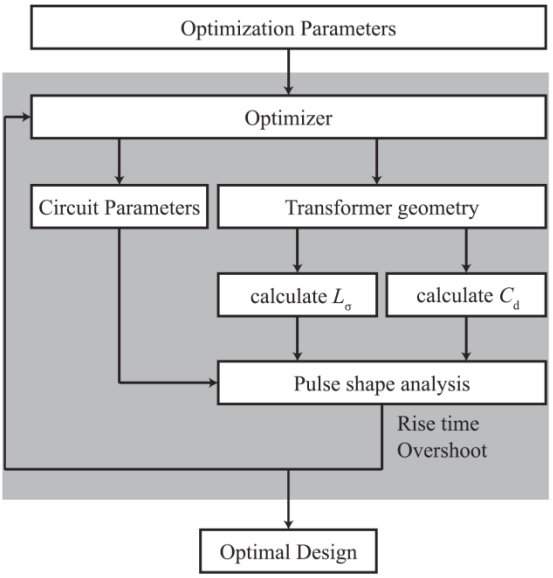


Fig.71 Flow chart for optimizing geometric parameters.

The damping factor, in the iterative process of *Fig.71*, can be modified by acting on one of four possible degrees of freedom. These are the height of the secondary winding h_w, the distance d_{w1}, the number of primary turns N_p, and an additional inductor on the primary side or secondary side. In addition at the above described action it is possible to increase the damping factor with the insertion of an additional inductor at the pulse generator by increasing the inductance L_{gen}

(*see paragraph* "***Pulse shape design***").

The second action envisaged by the project criterion under consideration is reduced the magnetic energy stored by the transformer or to use a pre-magnetization circuit. In fact, this circuit allows to halve the transverse section of the core. This further results in shorter winding lengths (lower copper losses), in a smaller volume between the windings (lower leakage inductance and distributed capacitance) and finally in a reduced rise time. Due to the higher core losses, however, a proper design concerning maximum allowable flux swing has to be done.

The flowchart that summarizes the procedures described above is shown in *Fig. 72* where the pulse transformer is designed not only to minimize energy losses but also and above all in meeting the pulse response requirements.

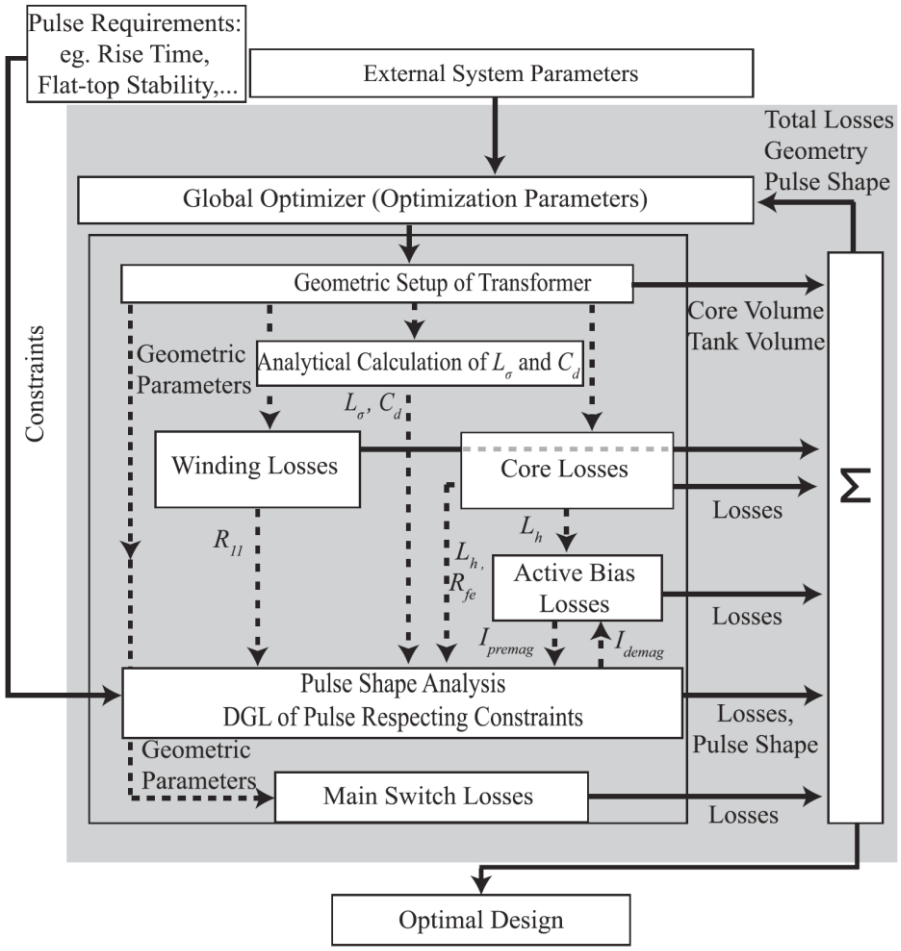


Fig. 72 Flowchart of the geometrical and external parameters optimization.

9 Conclusion

The design and implementation of a solid state pulse modulator is now one of the most difficult technological challenges of our times. Indeed, the demands of modulators impulsive able to operate at powers or at increasingly higher voltages requires the use of solutions to the limit of the technology. This is one of the reasons why the power semiconductor industry has developed devices in the last 50 years capable of operating at ever-increasing voltages and currents that can provide ever smaller response times.

In this paper we have tried to describe what today's technological solutions are to meet the increasingly demanding requirements of users (efficiency, pulse response, costs). Although the intention was to provide a useful guide to the design of pulse modulators based on the use of pulse transformers starting from a series of requirements on the transient response and the overall efficiency, it should be remembered at the most inexperienced designers that there are physical limits of applicability that must be evaluated by the context and the available technological solutions. In fact, for such a type of modulators, the limits are related to the physical feasibility of the pulse transformer and the charger unit to be assessed case by case.
Initially, the designer must consider whether:

- The specification on the response time of the impulse of the transformer is not antithetical with the requirement on the output voltage of the transformer for assigned overshoot;
- The energy requirement to accumulate in the charging unit to meet the droop voltage required for the output voltage is not excessively expensive and technologically impractical to achieve.

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